



(19)

Europäisches Patentamt
European Patent Office
Office européen des brevets



(11)

EP 0 887 850 A2

B ✓

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
30.12.1998 Bulletin 1998/53

(51) Int Cl.⁶: H01L 21/48, H01L 23/495

(21) Application number: 98304852.1

(22) Date of filing: 19.06.1998

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(72) Inventors:
• Hundt, Michael J.
Texas 75067 (US)
• Zhou, Tiao
Dallas, Texas 75063 (US)

(30) Priority: 23.06.1997 US 880566

(74) Representative: Palmer, Roger et al
PAGE, WHITE & FARRER
54 Doughty Street
London WC1N 2LS (GB)

(71) Applicant: STMicroelectronics, Inc.
Carrollton Texas 75006-5039 (US)

(54) Lead-frame forming for improved thermal performance

(57) A lead frame of a plastic integrated circuit package is fabricated in two steps. First, from a rectangular sheet of metal, lead fingers of the lead frame are formed. Second, the die pad of the lead frame is clamped and is simultaneously separated and downset from the lead fingers of the lead frame by shearing the lead frame with

a mated punch die pair. Performing the separation and downset of the die pad from the lead fingers results in essentially no horizontal gap between the lead fingers and the die pad. The downset of the die pad with respect to the lead fingers results in a vertical separation between the die pad and the lead fingers.

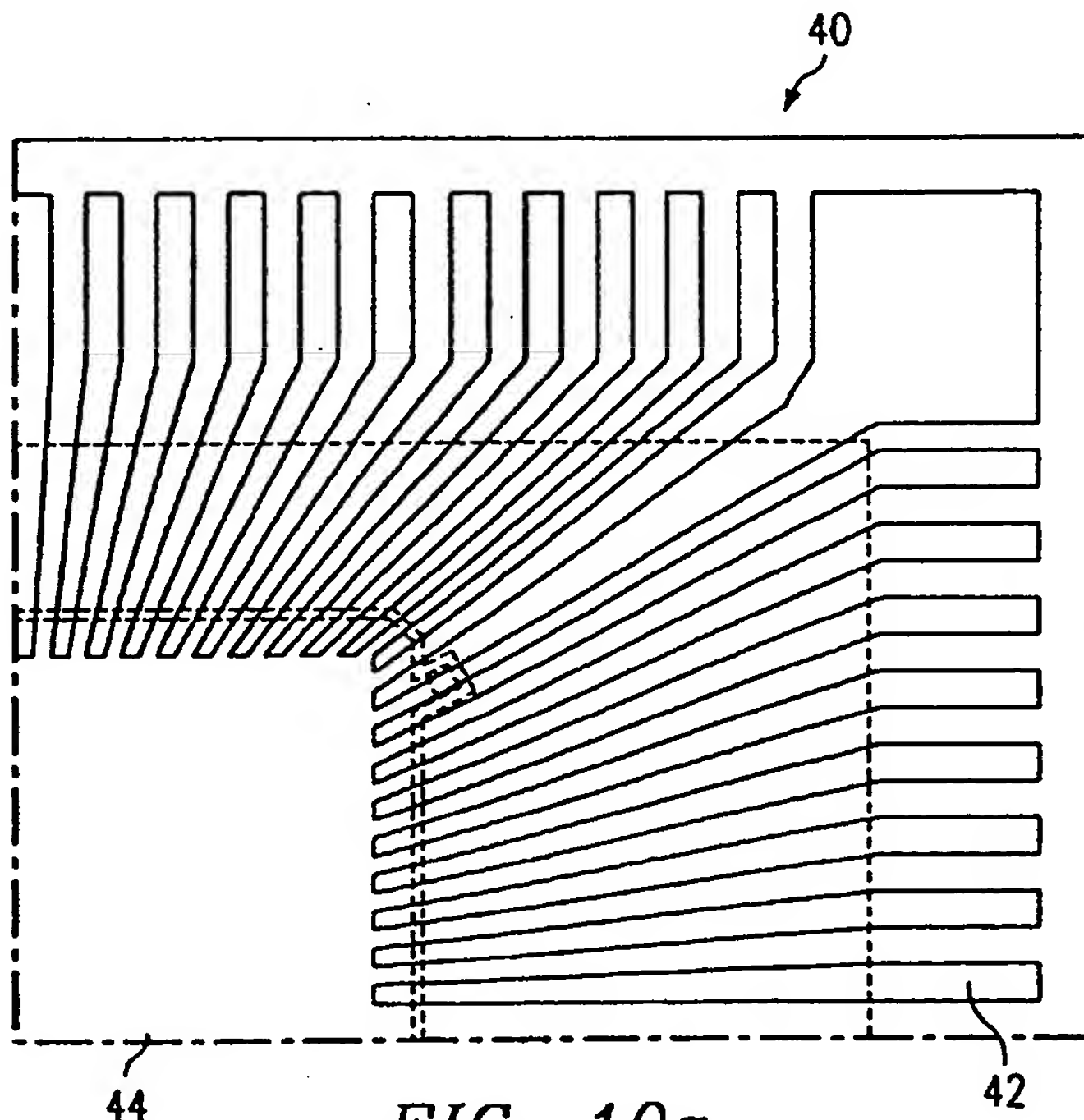
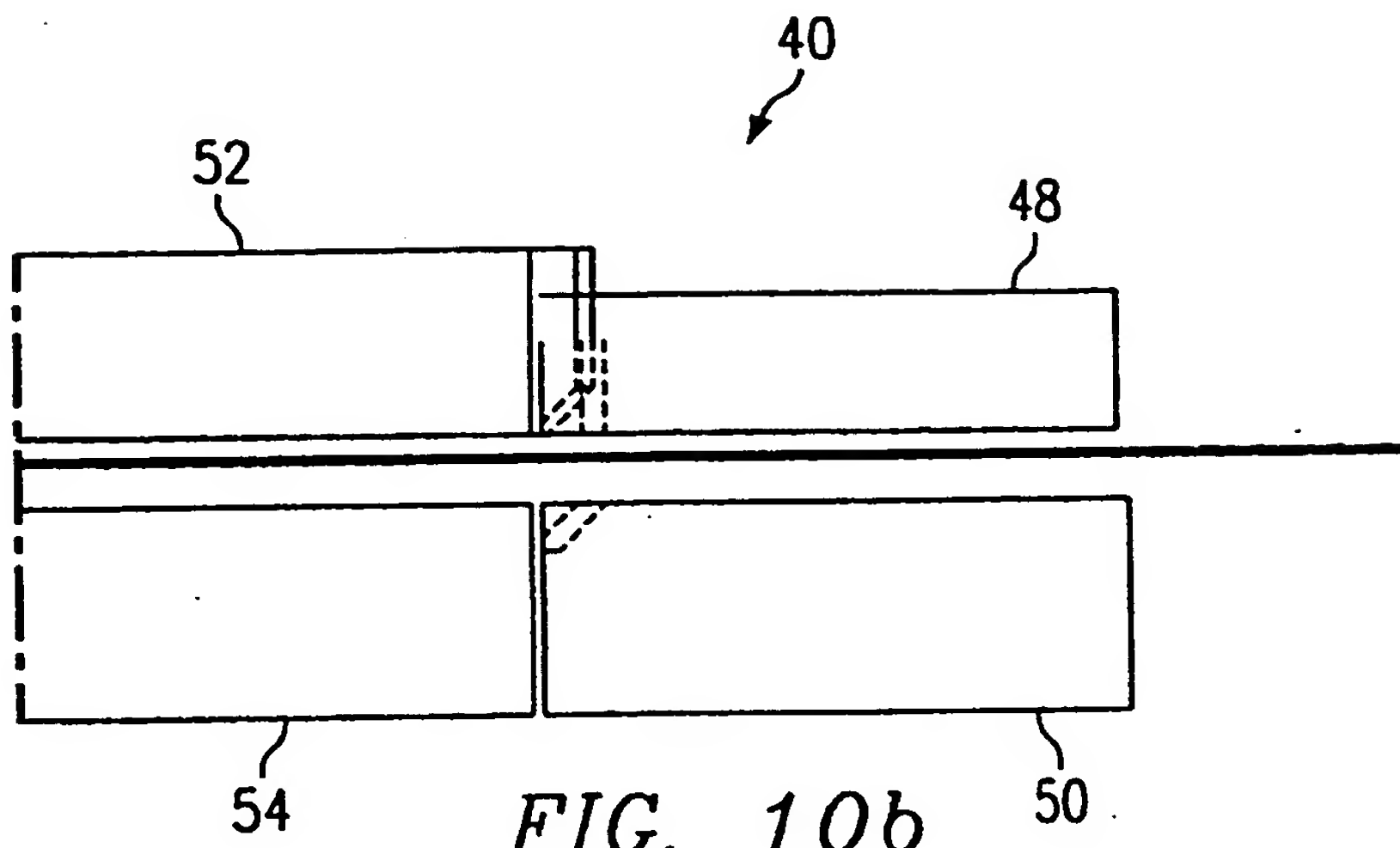


FIG. 10a

EP 0 887 850 A2



Description

The present invention relates generally to integrated circuit device packages, and more specifically to a plastic integrated circuit device package with a lead frame having improved thermal dissipation characteristics.

The trend in the electronics industry towards higher density integrated circuit devices has required that packages which house such higher density integrated circuit devices be able to dissipate more power. Because high density integrated circuit devices require more power and thus generate more heat, the manner in which the integrated circuit device package dissipates heat is critical. Generally speaking, it is quite advantageous to remove the heat from the integrated circuit device to the outside environment as quickly as possible.

The critical thermal path for removing heat from the integrated circuit device is defined as the path: (1) from the integrated circuit die to the die pad on which the integrated circuit die is seated, (2) from the die pad, by way of the horizontal air gap between the lead fingers and die pad, to the lead fingers of the lead frame, and (3) from the lead fingers to the printed circuit board on which the integrated circuit device is seated. Shortening this thermal path improves the thermal dissipation characteristics of the integrated circuit device package. As integrated circuit devices become more dense and thus must dissipate higher power, there is a continual need in the art to improve the heat dissipation characteristics of integrated circuit devices by shortening the thermal path of integrated circuit device packages.

A lead frame is the backbone of a molded plastic package. Lead frames are described in Chapter 8 of the 1989 edition of the Microelectronics Packaging Handbook (available from Van Nostrand Reinhold, 115 Fifth Avenue, New York, NY 10003). In general, a lead frame is fabricated from a strip of sheet metal by stamping or chemical milling. The lead frame serves first as a holding fixture during the assembly process, then, after molding, becomes an integral part of the package. A lead frame includes a plurality of finger-like connections that extend from the periphery of the lead frame toward a center die pad. A semiconductor or chip is mounted on the center die pad.

Lead frames are either chemically milled or mechanically stamped from rolled strip stock. Typical strip thickness is approximately 0.25 mm, with thinner material (of approximately 0.20 mm) used for high lead-count packages such as 84-pin PLCC and quad flat pacs. Chemical milling is a process that uses photolithography and metal-dissolving chemicals to etch a pattern from a metal strip.

Stamped lead frames are fabricated by mechanically removing metal from strip stock with tools called progressive dies. The energy required to shear metal is directly proportional to the length of shear. Lead frames have large shear lengths per unit area. Therefore, a

large amount of energy is required to stamp a full frame with one press stroke. Progressive dies are usually made of tungsten carbide and are arranged in stations. Each station punches a small area of metal from the strip as it moves through the die set.

To allow for the cutting tool, also known as a punch die, to be strong enough to operatively cut the lead frame, the prior art uses a cutting tool that has a narrow width of approximately 0.2 mil at the end increasing in width to a maximum width of approximately 30 to 40 mil at the base.

Referring to Figures 1a to 7b, the manufacturing process for fabricating a conventional lead frame 10 of a plastic integrated circuit package according to the prior art is illustrated. Fabrication begins with a rectangular sheet of metal from which the plurality lead fingers 12 of the lead frame are formed. Referring to Figure 1a, the top view of a quadrant of a lead frame 10 after the lead fingers 12 have been defined is shown. The plurality of lead fingers 12 are formed from a rectangular sheet of metal as is well known in the art. Figure 1b illustrates the cross-sectional view of the quadrant of the lead frame 10 at this stage of the process. The next step in the prior art process, as shown in the top view of Figure 2a, is to clamp the lead frame 10 into a fixed position prior to being cut with a punch die 22. Figure 2b illustrates the cross-sectional view of the quadrant of the lead frame 10, the upper clamp 18 and lower clamp 20, and the punch die 22. The next step in the prior art process, as shown in the top view of Figure 3a, is to separate the lead fingers 12 from the die pad 14 of the lead frame. At a substantially central portion of the lead frame 10, a square die pad 14, configured for mounting a semiconductor or chip thereon, supported by a plurality of suspension tie bars 16 is formed by cutting the lead frame 10 with the punch die 22. The punch die 22 having a plurality of recesses along the cutting surface forming the plurality of tie bars 16 as the lead frame 10 is cut. Figure 3b illustrates the cross-sectional view of the quadrant of the lead frame, the upper clamp 18 and lower clamp 20, and the punch die 22 after the lead frame 10 is cut with the punch die 22. Tie bars 16 connect lead fingers 12 to die pad 14. Figure 4a is a top view of a quadrant of the lead frame after the lead frame has been cut with a punch die 22 showing the physical separation between the lead fingers and the die pad 14. Figure 4b illustrates the cross-sectional view of the quadrant of the lead frame at this stage of the process. Figure 5 is a top view of the lead frame after the top and bottom portions of the lead frame have been cut with a punch die 22. Figure 6a and 6b illustrate the lead frame showing the physical separation between the lead fingers 12 and the die pad 14. The plurality of lead fingers 12 extend from the periphery of the lead frame 10 to a position spaced apart from the die pad 14 with a predetermined distance represented as $\Delta > 0$, where Δ is defined as the horizontal gap between the lead fingers 12 and the die pad 14. It is also clear that the lead fingers 12 and the die pad

14 are co-planar at this stage of the fabrication process. Referring to Figures 7a and 7b, the last step of the process is to downset the die pad 14 in relation to the lead fingers 12. In performing the downset, it is noted that the physical separation between the lead fingers 12 and the die pad 14, represented as $\Delta 0$, is maintained. Additionally, the downset of die pad 14 results in a vertical separation between lead fingers 12 and die pad 14.

Referring to Figure 8, the fabrication of the lead frame of a plastic integrated circuit package, according to the prior art, is illustrated in process flow 30. First, the lead frame begins as a flat metal sheet as shown in step 32. Next, at step 34, the lead fingers 12 are defined. Step 34 corresponds to Figures 1a and 1b. After the lead fingers 12 are defined, they are separated from the die pad 14 in step 36. Step 36 corresponds to Figures 3a and 3b. Finally, at step 38, the die pad 14 is downset with respect to the lead fingers 12 as illustrated in Figures 7a and 7b.

According to the lead frame formed in Figures 1-8, the critical thermal path by which heat must be dissipated is defined as the distance from the integrated circuit die to the downset die pad 14 on which the integrated circuit die is placed; from the die pad 14, by way of the horizontal air gap Δ between the lead fingers 12 and die pad 14, to lead fingers 12; and from lead fingers 12 to the printed circuit board on which the integrated circuit device is placed. Shortening this thermal path would improve the thermal dissipation characteristics of the integrated circuit device. There is therefore an unmet need in the art to shorten the critical thermal path of the prior art lead frame used in plastic integrated circuit device packages.

It is therefore an object of the present invention to shorten the critical thermal path of the prior art lead frame used in plastic integrated circuit device packages.

Therefore, according to a preferred embodiment of the present invention, a process for fabricating a lead frame of a plastic integrated circuit package is disclosed. Fabrication begins with a rectangular sheet of metal from which the plurality lead fingers of the lead frame are formed as is well known in the art. Next, the lead frame is clamped into a fixed position. Finally, the die pad of the lead frame is simultaneously separated and downset from the lead fingers of the lead frame by shearing the lead frame with a punch die pair. At a substantially central portion of the lead frame, a square die pad, configured for mounting a semiconductor or chip thereon, supported by a plurality suspension tie bars is formed by shearing the lead frame with a punch die pair and a lower clamp that are mated such that the punch die pair may be inserted into the lower clamp with essentially a negligible gap of no more than 2 percent of the lead frame thickness. The punch die pair having 90 degree cutting surfaces and a plurality of recesses along the cutting surfaces forming the plurality tie bars as the lead frame is sheared. Tie bars connect lead fingers to the die pad. Performing the separation and downset of

the die pad from the lead fingers results in essentially no horizontal gap between the lead fingers and the die pad. However, the downset of the die pad with respect to the lead fingers does result in a vertical separation between the die pad and the lead fingers that was also seen in the prior art. The separation and downset step may be accomplished by a simultaneous cutting and pressing operation resulting in the lead frame being sheared.

The lead frame of the preferred embodiment of the present invention has a shorter critical thermal path than the prior art lead frame since there is essentially no horizontal gap between the lead fingers and the die pad of the lead frame, unlike the prior art lead frame. The shorter critical thermal path means that the lead frame is much more efficient at dissipating the heat generated by high density integrated circuit devices.

According to an alternate embodiment of the present invention, the step of simultaneously separating and downsetting the die pad with respect to the lead fingers of the lead frame may be separated into two steps. First, the lead fingers are separated from the die pad using a cutting tool, such as a laser, that results in essentially no horizontal gap. Second, the die pad is downset with respect to the lead fingers. There is the vertical gap between the lead fingers and the die pad caused by the downset of die pad. The alternate process of forming the lead frame still provides the advantage of shortening the critical thermal path of the lead frame and therefore improves the thermal dissipation characteristics of any plastic integrated circuit device package into which it is placed. However, the alternate embodiment has more process steps than does the preferred embodiment.

These and other objects of the invention will become apparent from the detailed description of the invention in which numerals used throughout the description correspond to those found in the drawing figures.

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1a is a top view of a quadrant of a lead frame after the lead fingers have been defined, according to the prior art;

Figure 1b is a cross-sectional view of the quadrant of the lead frame of Figure 1a, according to the prior art;

Figure 2a is a top view of a quadrant of the lead frame after the lead frame has been clamped, according to the prior art;

Figure 2b is a cross-sectional view of the quadrant of the lead frame of Figure 2a, according to the prior art;

Figure 3a is a top view of a quadrant of the lead frame after the lead frame has been cut with a punch die, according to the prior art;

Figure 3b is a cross-sectional view of the quadrant of the lead frame of Figure 3a, according to the prior art;

Figure 4a is a top view of a quadrant of the lead frame after the lead frame has been cut with a punch die showing the physical separation between the lead fingers and the die pad, according to the prior art;

Figure 4b is a cross-sectional view of the quadrant of the lead frame of Figure 4a, according to the prior art;

Figure 5 is a top view of the lead frame after the top and bottom portions of the lead frame have been cut with a punch die, according to the prior art;

Figure 6a is a top view of the lead frame after the lead fingers have been separated from the die pad, according to the prior art;

Figure 6b is a cross-sectional view of the lead frame of Figure 6a, according to the prior art;

Figure 7a is a top view of the lead frame after the die pad has been downset with respect to the lead fingers of the lead frame, according to the prior art;

Figure 7b is a cross-sectional view of the lead frame of Figure 7a, according to the prior art;

Figure 8 is the process flow for fabricating a lead frame of a plastic integrated circuit package, according to the prior art;

Figure 9a is a top view of a quadrant of a lead frame after the lead fingers have been defined, according to the present invention;

Figure 9b is a cross-sectional view of the quadrant of the lead frame of Figure 9a, according to the present invention;

Figure 10a is a top view of a quadrant of the lead frame after the lead frame has been clamped, according to the present invention;

Figure 10b is a cross-sectional view of the quadrant of the lead frame of Figure 10a, according to the

present invention;

Figure 11 is a top view a lead frame after the lead frame has been clamped, according to the present invention;

Figure 12a is a top view of a quadrant of the lead frame after the lead frame has been simultaneously cut and downset with a punch die pair, according to the present invention;

Figure 12b is a cross-sectional view of the quadrant of the lead frame of Figure 12a, according to the present invention;

Figure 13 is a top view of the lead frame after the lead frame has been simultaneously cut and downset with a punch die pair, according to the present invention;

Figure 14a is a top view of a quadrant of the lead frame after the lead frame has been unclamped, according to the present invention;

Figure 14b is a cross-sectional view of the quadrant of the lead frame of Figure 14a showing a tie bar after the die pad has been downset with respect to the lead fingers of the lead frame, according to the present invention;

Figure 15 is a blow-up cross-sectional view of the lead frame showing a tie bar after the die pad has been downset with respect to the lead fingers of the lead frame, according to the present invention; and

Figure 16 is the process flow for fabricating a lead frame of a plastic integrated circuit package, according to a preferred embodiment of the present invention.

Effective thermal enhancement of an integrated circuit device may be obtained by shortening its critical thermal path. A cost effective solution is to reduce the distance from the die pad to the lead gap in the lead frame forming process. Minimizing the distance from the die pad to the lead fingers will result in superior thermal performance for plastic integrated circuit device packages, including Plastic Quad Flat Pack (PQFP) packages, compared to traditional lead frame manufacturing processes.

Referring to Figures 9a to 15, the manufacturing process for fabricating a lead frame of a plastic integrated circuit package according to the present invention is illustrated. As in the prior art, fabrication begins with a rectangular sheet of metal from which the lead fingers of the lead frame are formed. Referring to Figure 9a, the top view of a quadrant of a lead frame 40 after the lead fingers 42 have been defined is shown. The plural-

ity of lead fingers 12 are formed from a rectangular sheet of metal as is well known in the art. Figure 9b illustrates the cross-sectional view of the quadrant of the lead frame at this stage of the process. Next, as shown in Figure 10a, the top view of a quadrant of the lead frame 40, is to clamp the lead frame 40 into a fixed position prior to being simultaneously cut and downset with a punch die pair. Figure 10b illustrates the cross-sectional view of the quadrant of the lead frame, the upper clamp 48 and lower clamp 50, and the upper punch die 52 and lower punch die 54. Figure 11 shows the top view of the entire lead frame 40 at this stage of the process. The last step in the present invention process, as shown in Figures 12a-15, is to simultaneously separate the lead fingers 42 from die pad 44 and downset the die pad 44 with respect to the lead fingers 42 by shearing the lead frame with a punch die pair. At a substantially central portion of the lead frame 40, a square die pad 44, configured for mounting a semiconductor or chip thereon, supported by a plurality suspension tie bars 46 is formed by shearing the lead frame 40 with a punch die pair and a lower clamp 50 that are mated such that the punch die pair may be inserted into the lower clamp 50 with essentially a 0 gap of no more than 2 percent of the lead frame 40 thickness. The punch die pair having 90 degree cutting surfaces and a plurality of recesses along the cutting surfaces forming the plurality tie bars as the lead frame 40 is sheared. As shown in the cross-sectional view of Figure 15, performing the separation and downset of die pad 44 from lead fingers 42 results in essentially no horizontal gap between lead fingers 42 and die pad 44. However, the downset of die pad 44 with respect to lead fingers 42 results in a vertical separation between die pad 44 and lead fingers 42 that was also seen in the prior art. The separation and downset step may be accomplished by a simultaneous cutting and pressing operation. During the downset step, tie bar 46 is angled downward connecting lead fingers 42 to die pad 44.

Referring to Figure 16, the fabrication of the lead frame of a plastic integrated circuit package, according to the present invention, is illustrated in process flow 60. First, the lead frame begins as a flat metal sheet as shown in step 62. Step 62 corresponds to Figures 9a and 9b. Next, at step 64, the lead fingers 42 are defined. In the next and final step of the process, the die pad 44 is simultaneously separated and downset from lead fingers 42. Step 64 results in the vertical gap between the lead fingers 42 and die pad 44 with no horizontal gap. Step 64 corresponds to Figures 12a-15.

The preferred embodiment of the present invention describes a process for forming a lead frame of a plastic integrated circuit device package. The resultant lead frame has a shorter critical thermal path than the prior art lead frame since there is no horizontal gap between the lead fingers and the die pad of the lead frame, unlike the prior art lead frame. The shorter critical thermal path means that the lead frame is much more efficient at dis-

sipating the heat generated by high density integrated circuit devices.

The process for forming the lead frame only requires two steps. First, the lead fingers are defined from the flat metal sheet as shown in Figure 9a and Step 64 of Figure 16. Second, the die pad is clamped as shown in Figures 10a-11 and is simultaneously separated and downset with respect to the lead fingers as shown in Figures 12a-15 and Step 66 of Figure 16.

According to an alternate embodiment of the present invention, the step of simultaneously separating and downsetting the die pad with respect to the lead fingers of the lead frame may be separated into two steps. First, the lead fingers 42 are separated from the die pad 44 using a cutting tool, such as a laser, that results in essentially no horizontal gap. Second, the die pad 44 is downset with respect to the lead fingers 42. The resultant lead frame is the same as illustrated in Figures 10 and 11. There is no horizontal gap between the lead fingers 42 and die pad 44. There is a vertical gap between the lead fingers 42 and die pad 44 caused by the downset of die pad 44.

The alternate embodiment process for forming the lead frame would still provide the advantage of shortening the critical thermal path of the lead frame and therefore improve the thermal dissipation characteristics of any plastic integrated circuit device package into which it is placed.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

Claims

1. A method for fabricating a lead frame of a plastic integrated circuit device package, comprising:

defining a plurality of lead fingers of the lead frame; and

simultaneously separating a die pad of the lead frame from the plurality of lead fingers and downsetting the die pad from the plurality of lead fingers to produce a vertical separation between the die pad and the plurality of lead fingers, wherein separating the die pad from the plurality of lead fingers results in essentially no horizontal gap between the die pad and the plurality of lead fingers.

2. A method for fabricating a lead frame of a plastic integrated circuit device package, comprising:

defining a plurality of lead fingers of the lead

frame;

separating a die pad of the lead frame from the plurality of lead fingers, wherein separating the die pad from the plurality of lead fingers results in essentially no horizontal gap between the die pad and the plurality of lead fingers; and 5

downsetting the die pad from the plurality of lead fingers to produce a vertical separation between the die pad and the plurality of lead fingers. 10

3. A lead frame of an integrated circuit device package, comprising: 15

a plurality of lead fingers; and

a die pad, wherein the die pad is separated from the plurality of lead fingers with essentially no horizontal gap between the die pad and the plurality of lead fingers. 20

4. The structure of claim 3, wherein the die pad is an octagonal shape. 25

5. The structure of claim 3, wherein the integrated circuit device package is plastic.

6. The structure of claim 3, wherein the die pad is downset from the plurality of lead fingers defining a vertical separation between the die pad and the plurality of lead fingers. 30

7. The structure of claim 6, wherein the die pad has an octagonal shape. 35

40

45

50

55

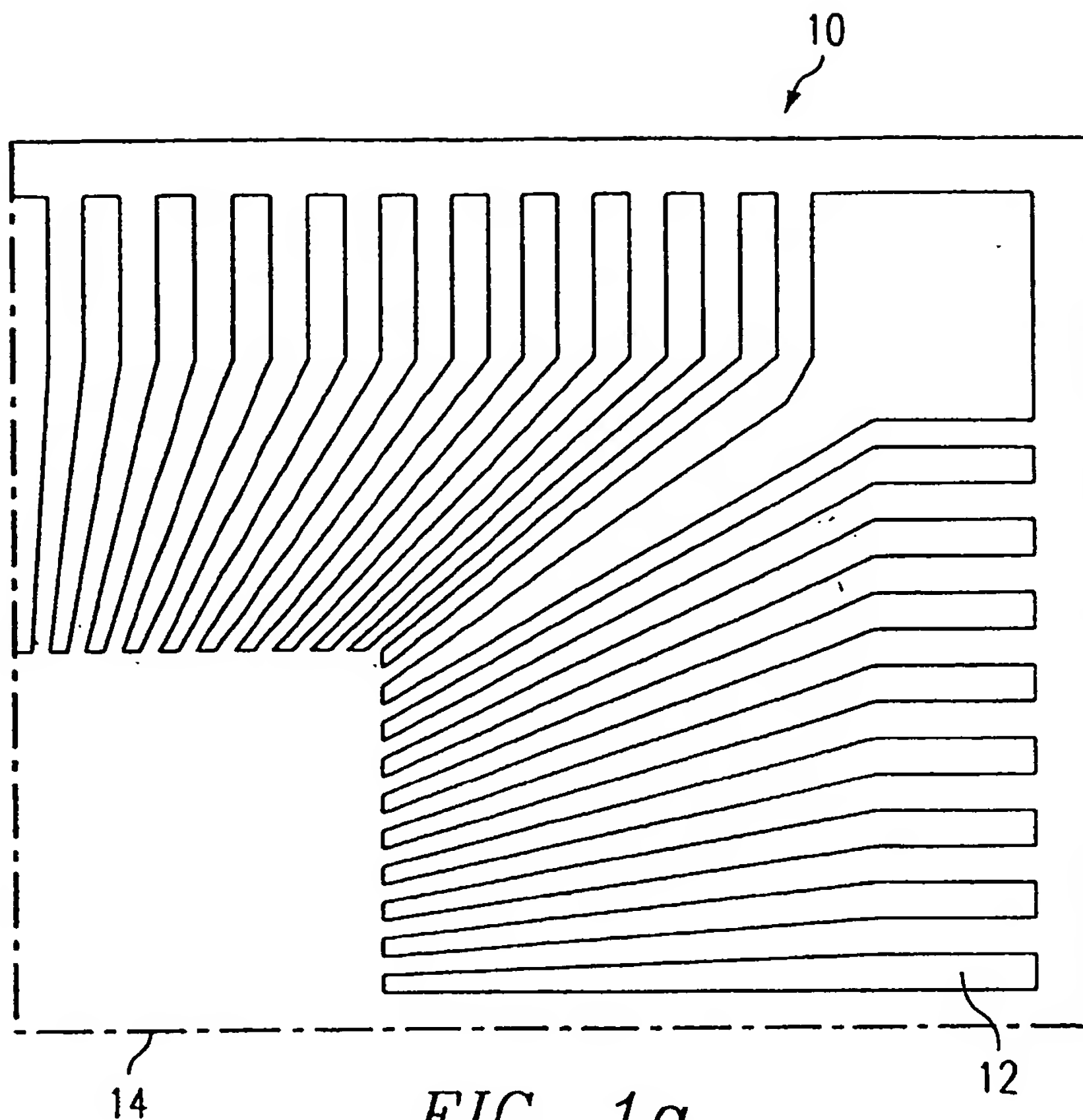


FIG. 1a
(PRIOR ART)



FIG. 1b
(PRIOR ART)

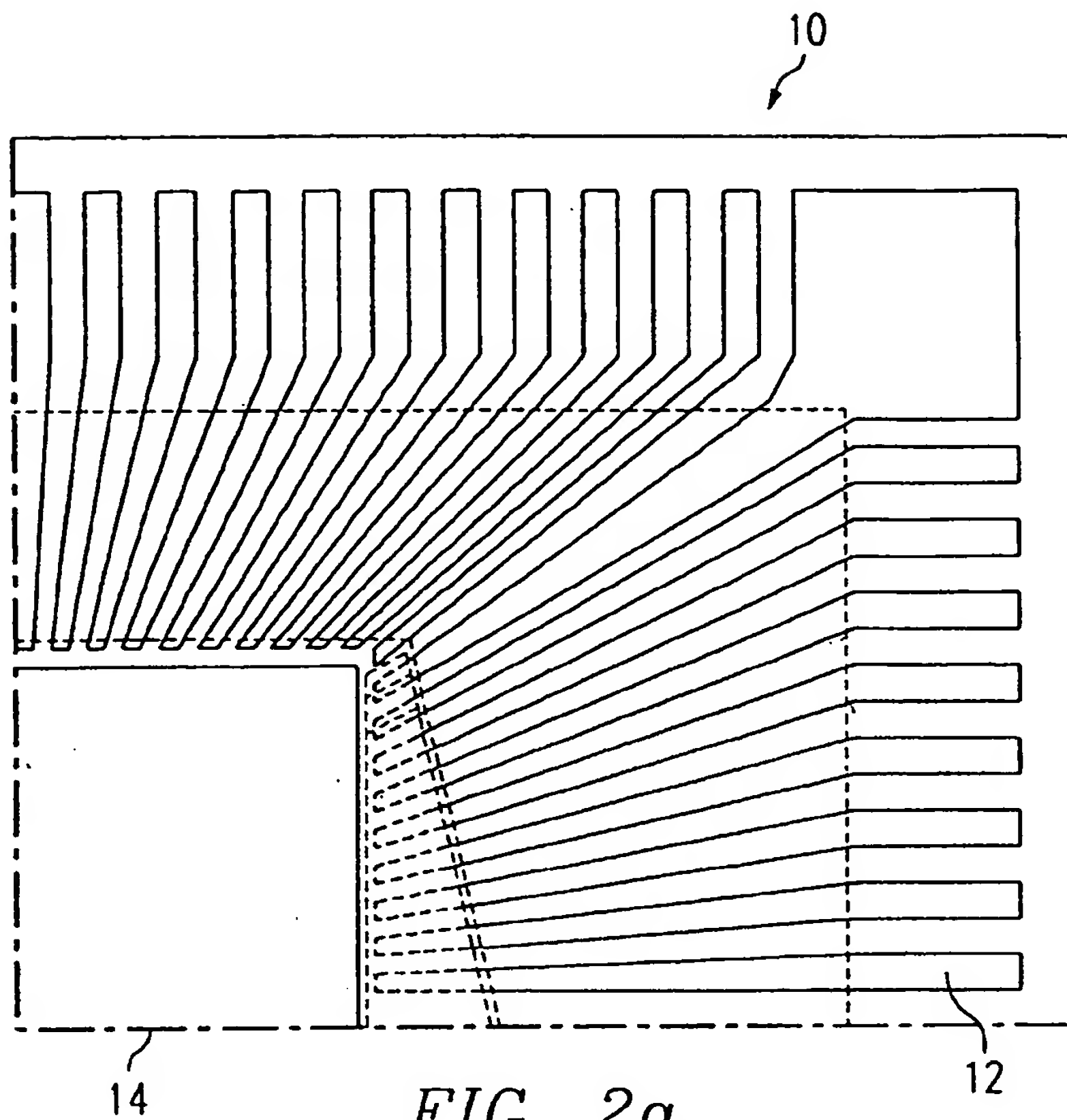


FIG. 2a
(PRIOR ART)

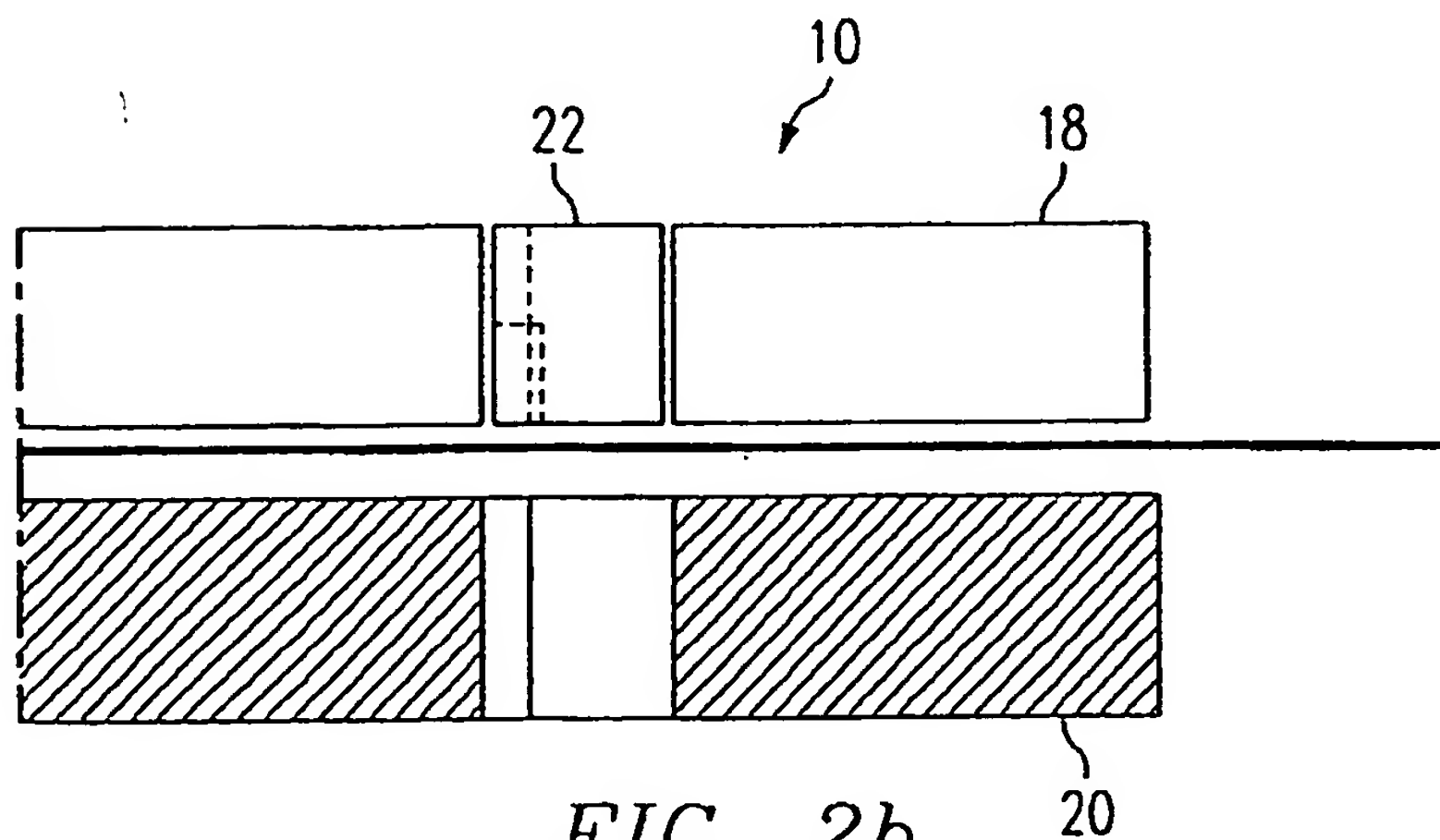
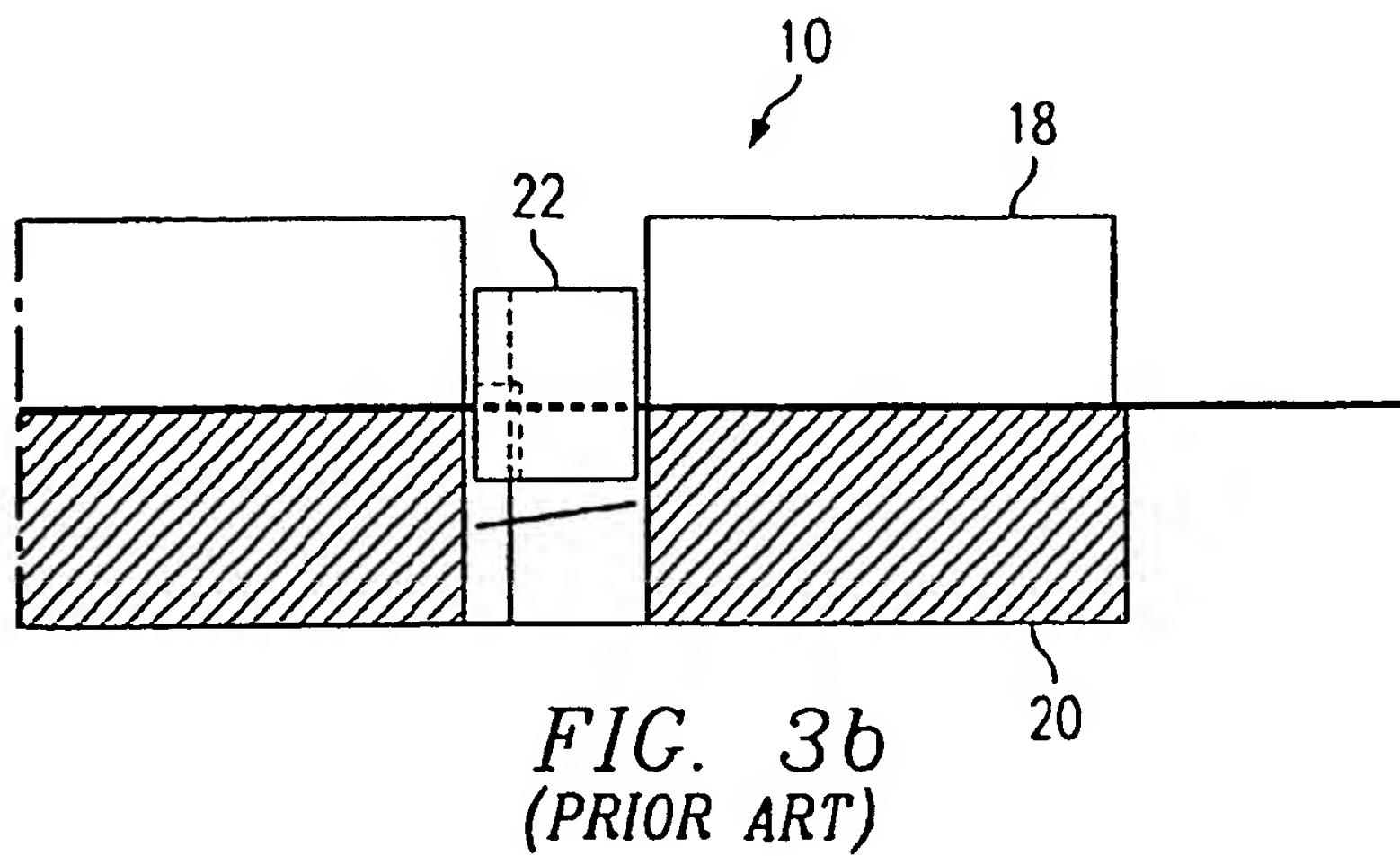
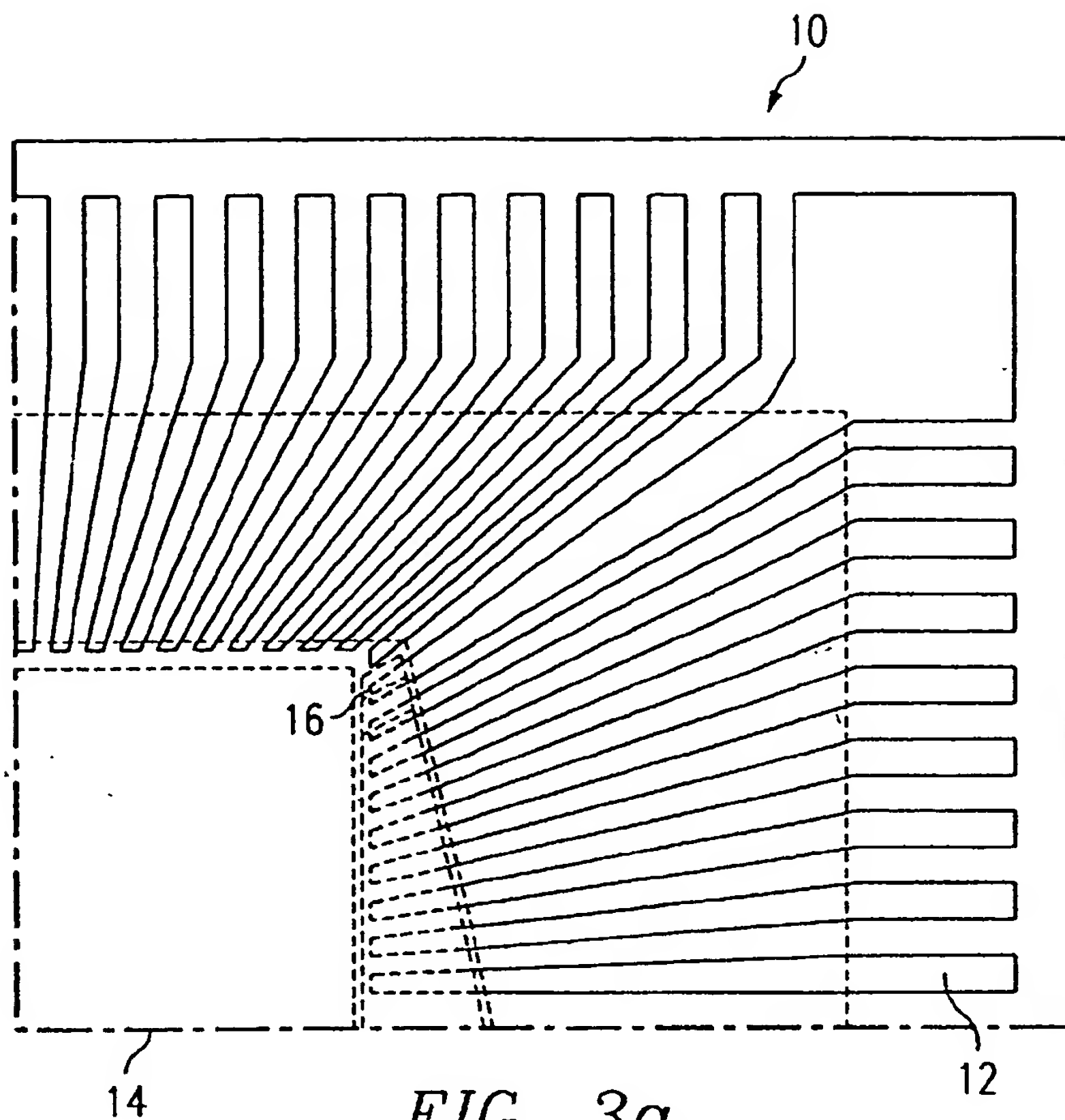


FIG. 2b
(PRIOR ART)



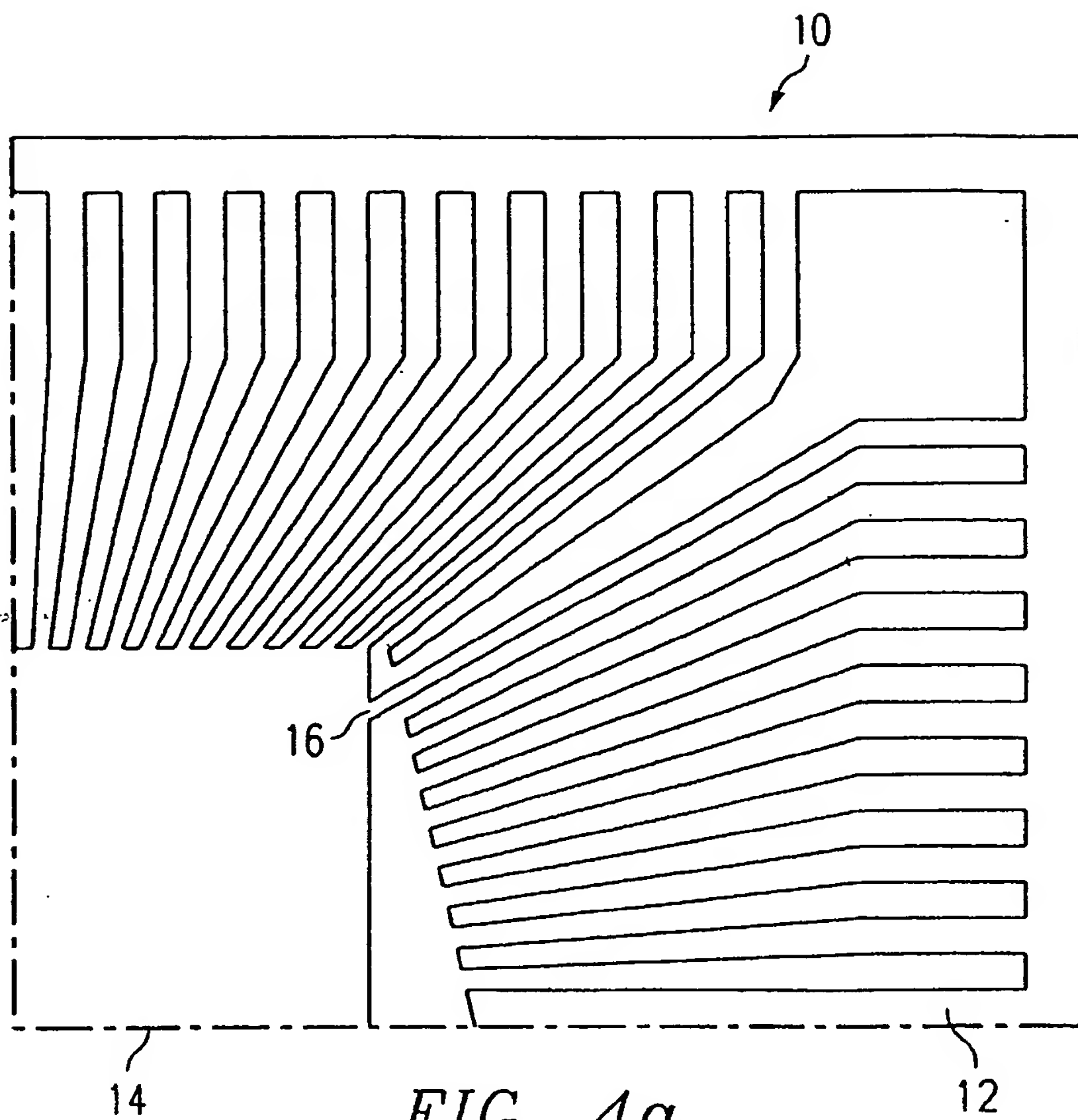


FIG. 4a
(PRIOR ART)



FIG. 4b
(PRIOR ART)

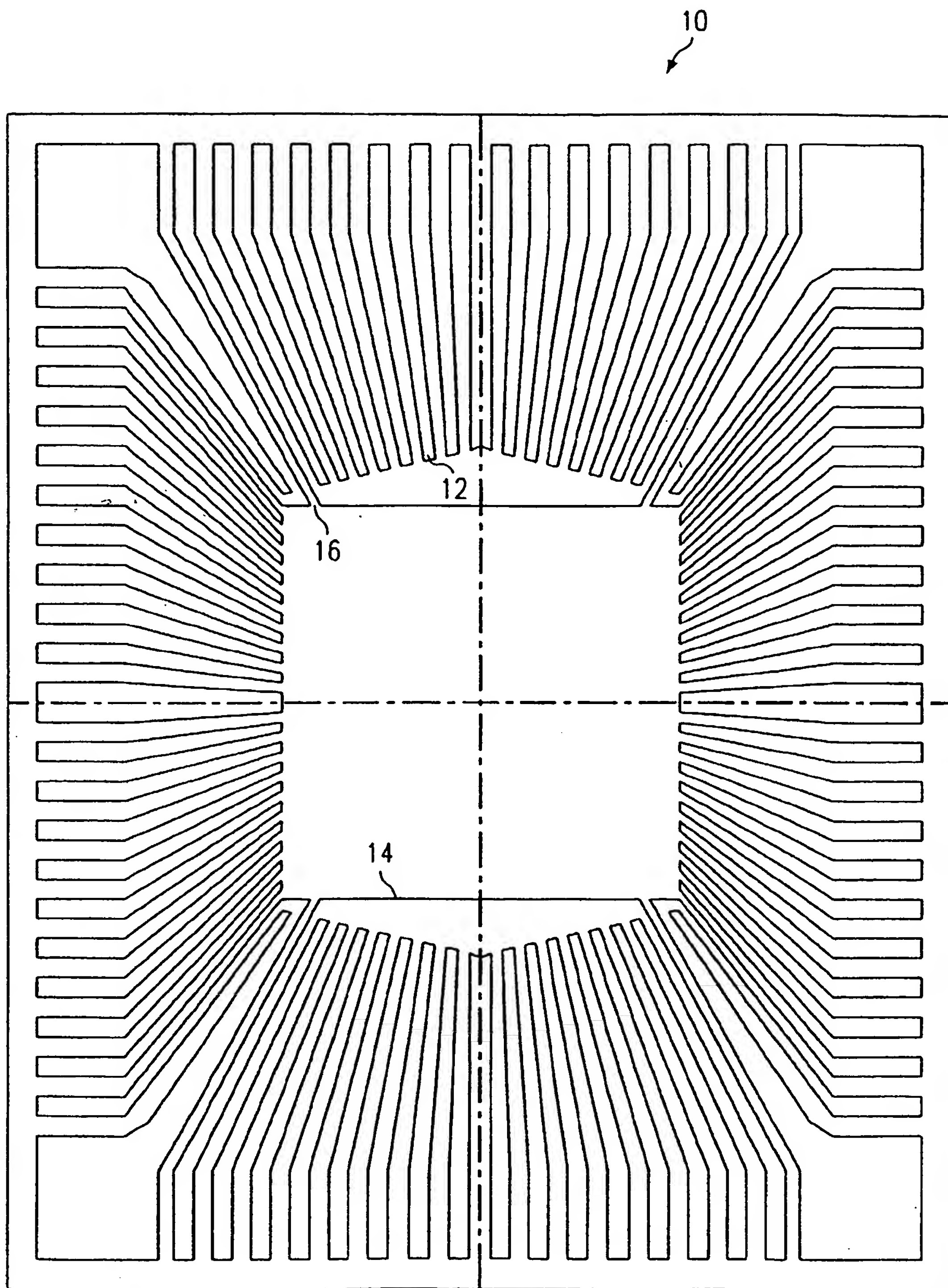


FIG. 5
(PRIOR ART)

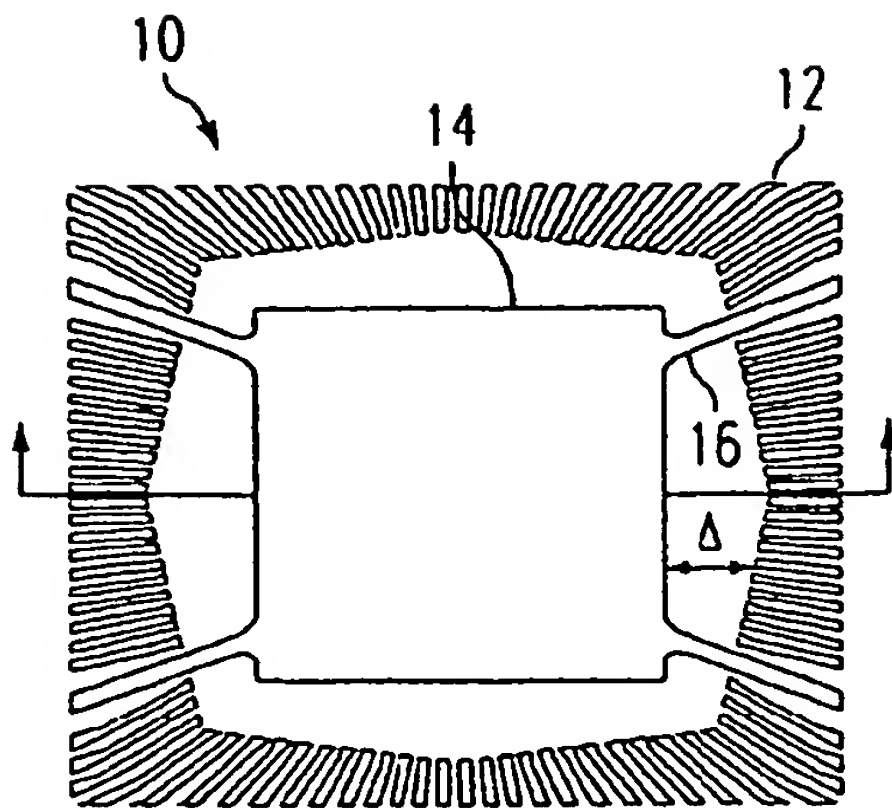


FIG. 6a
(PRIOR ART)

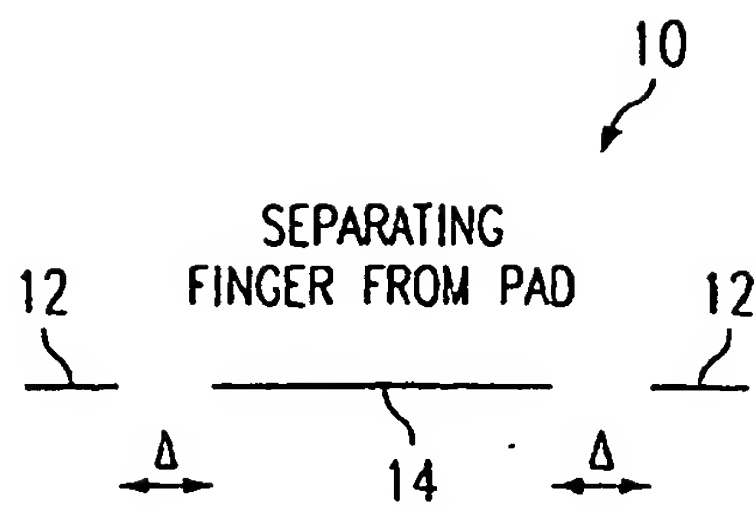


FIG. 6b
(PRIOR ART)

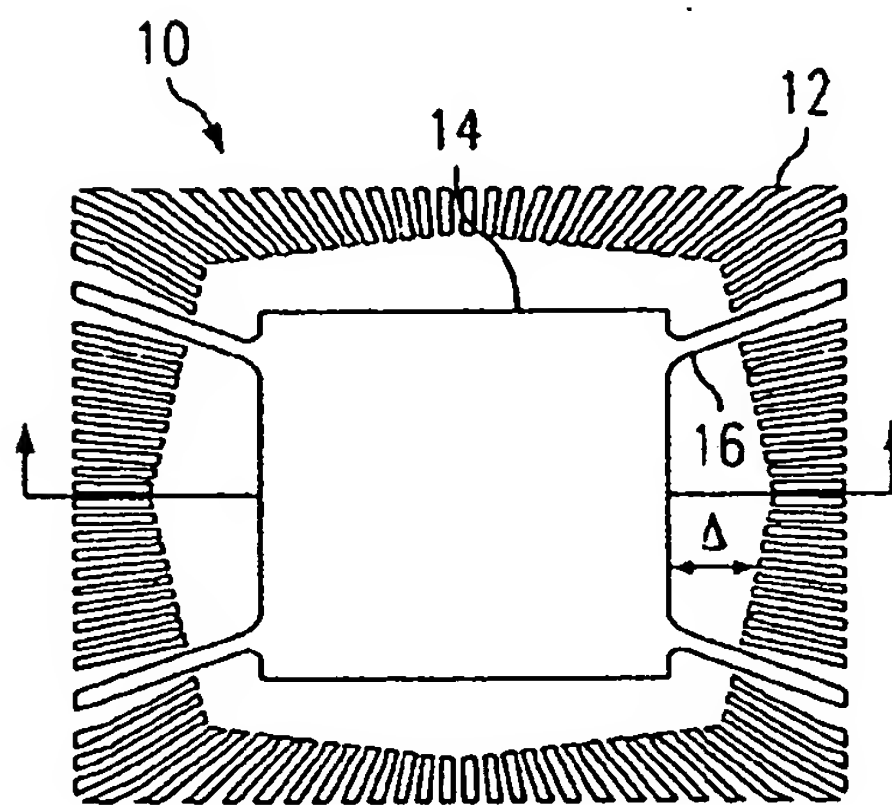


FIG. 7a
(PRIOR ART)

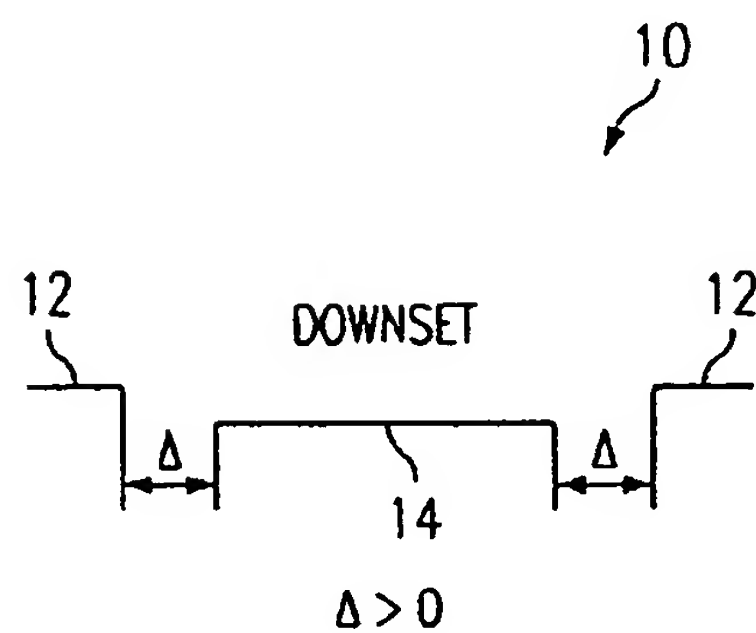


FIG. 7b
(PRIOR ART)

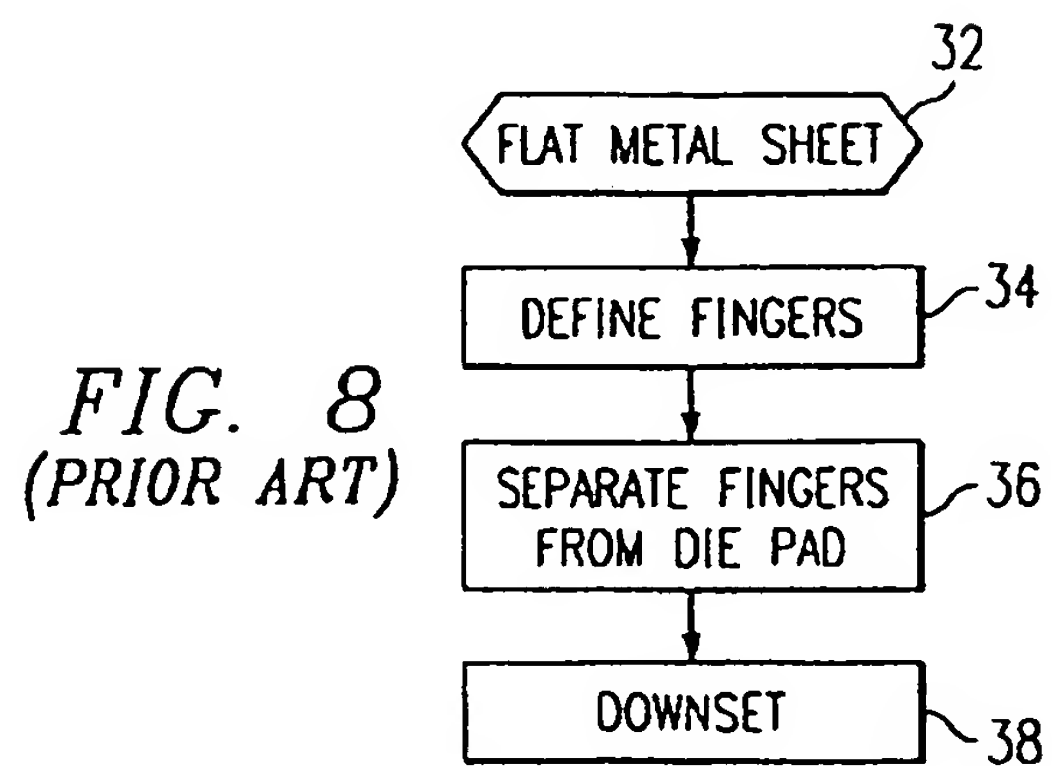


FIG. 8
(PRIOR ART)

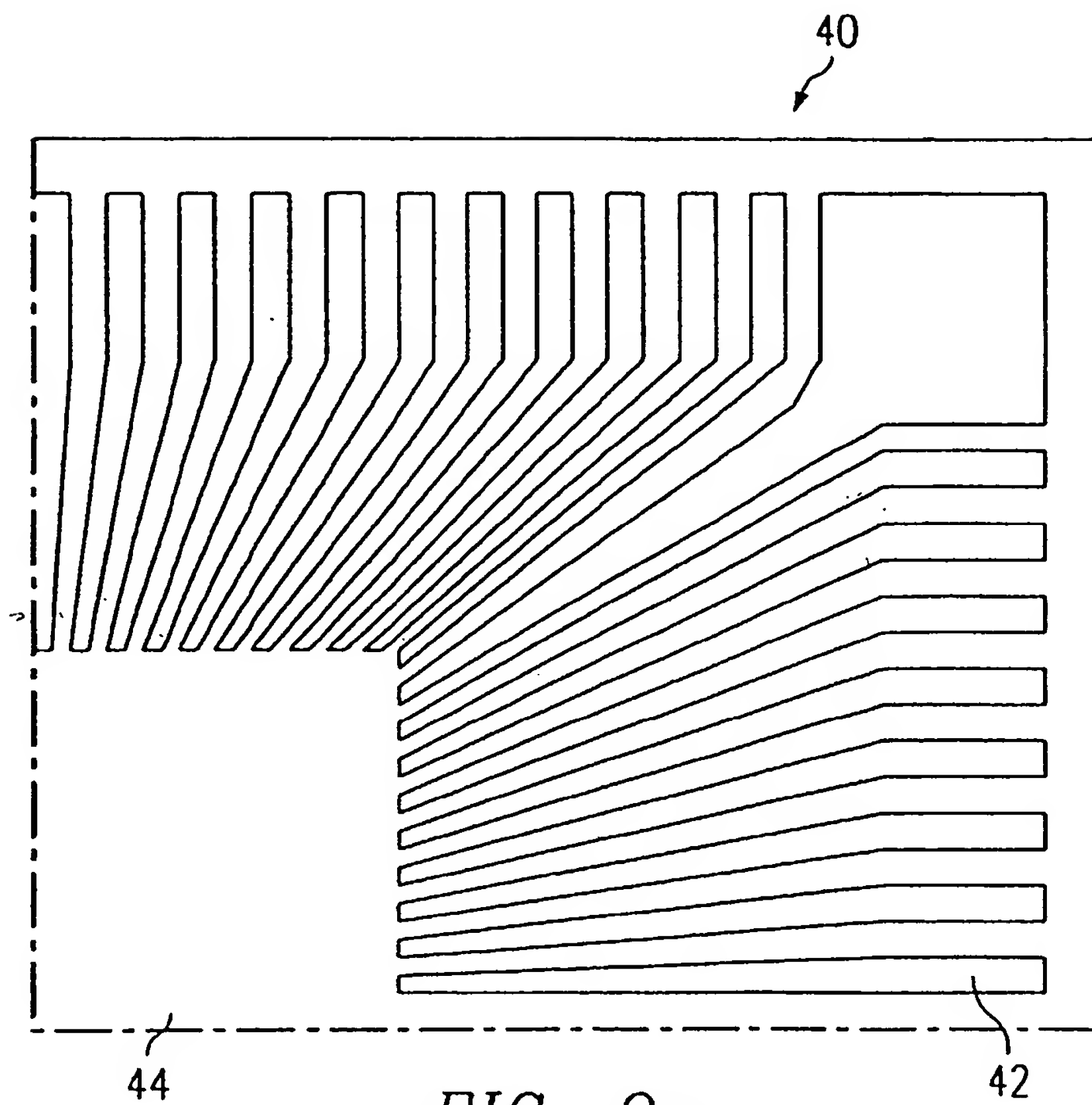
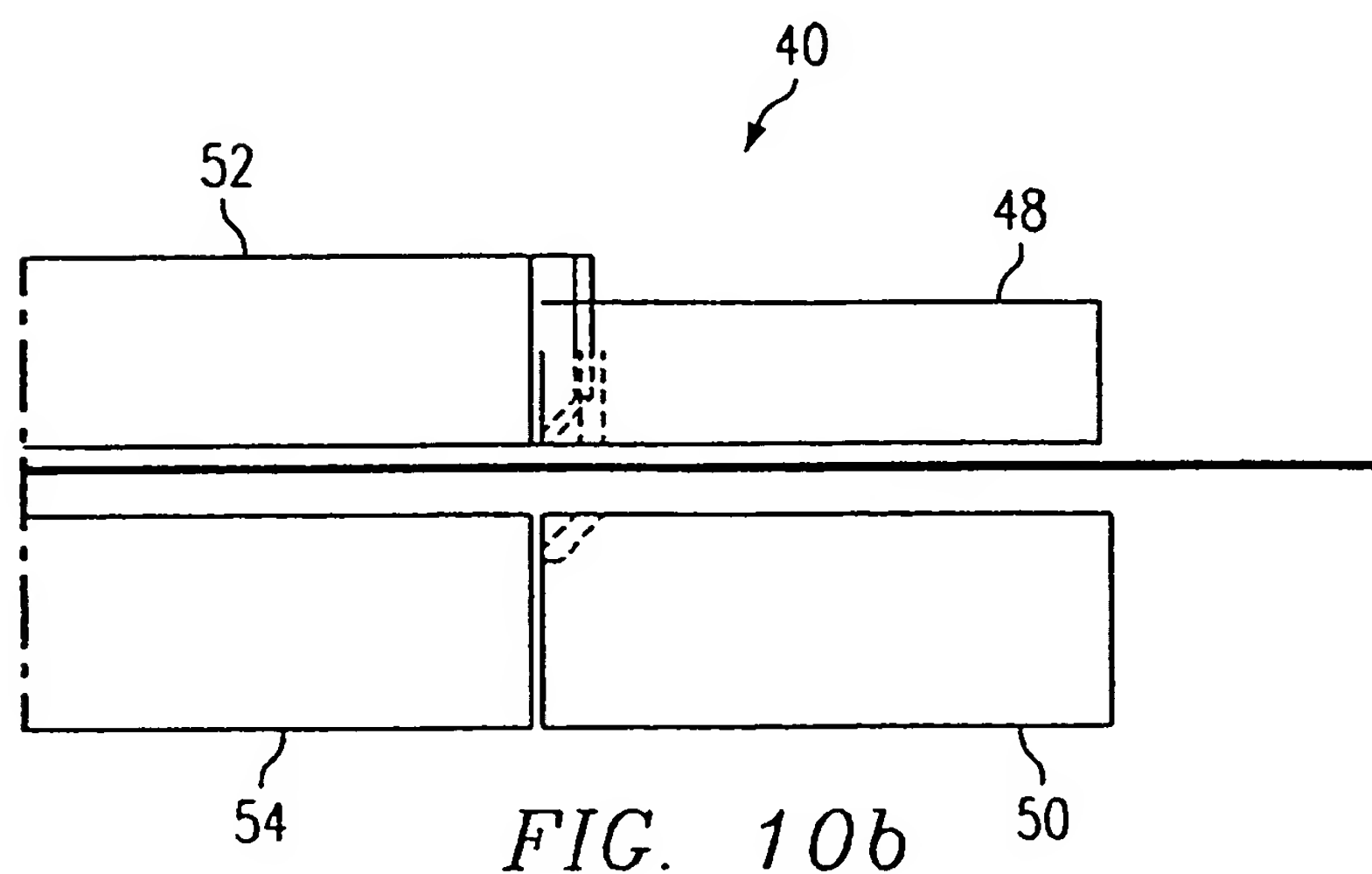
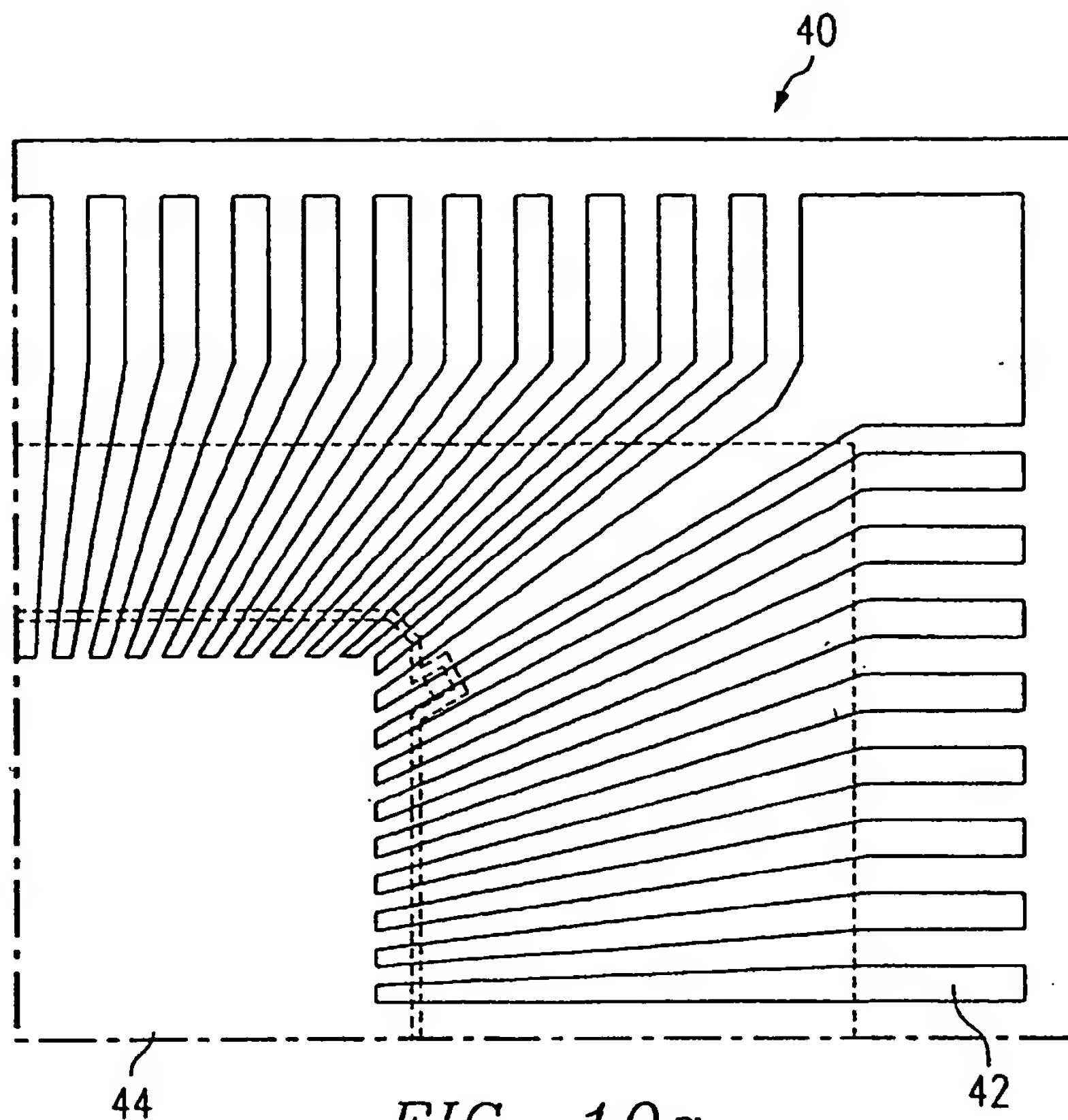


FIG. 9a



FIG. 9b



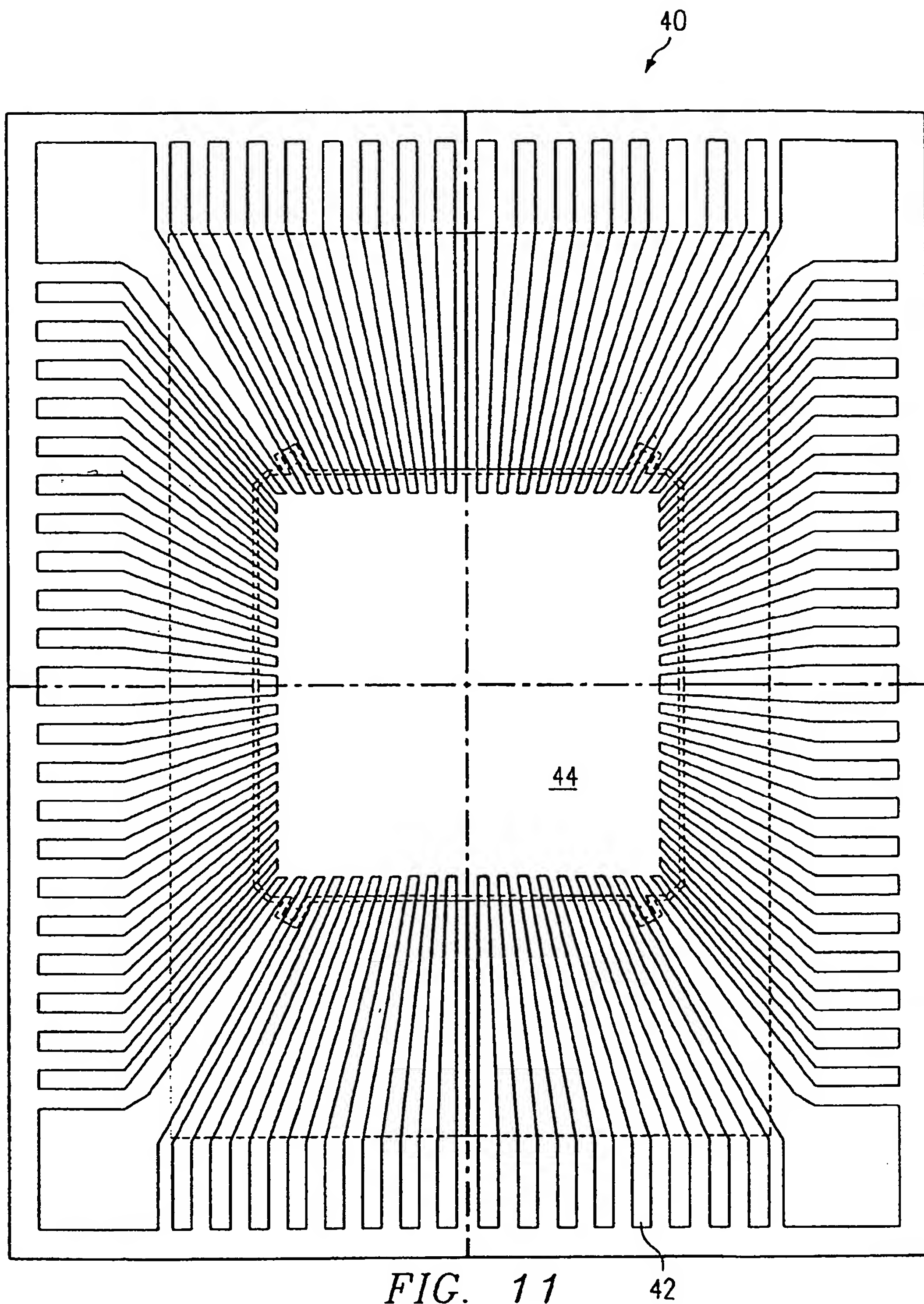
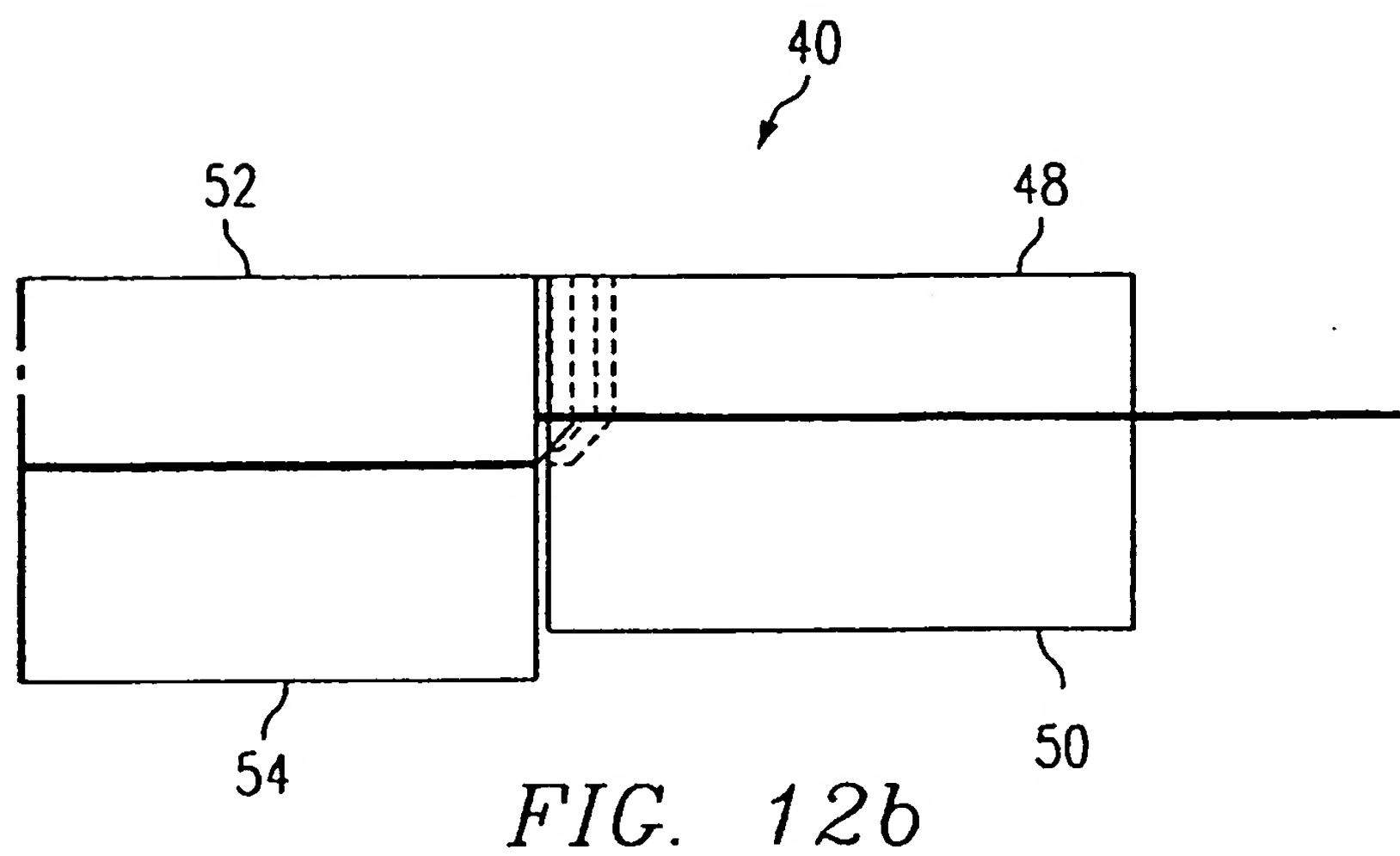
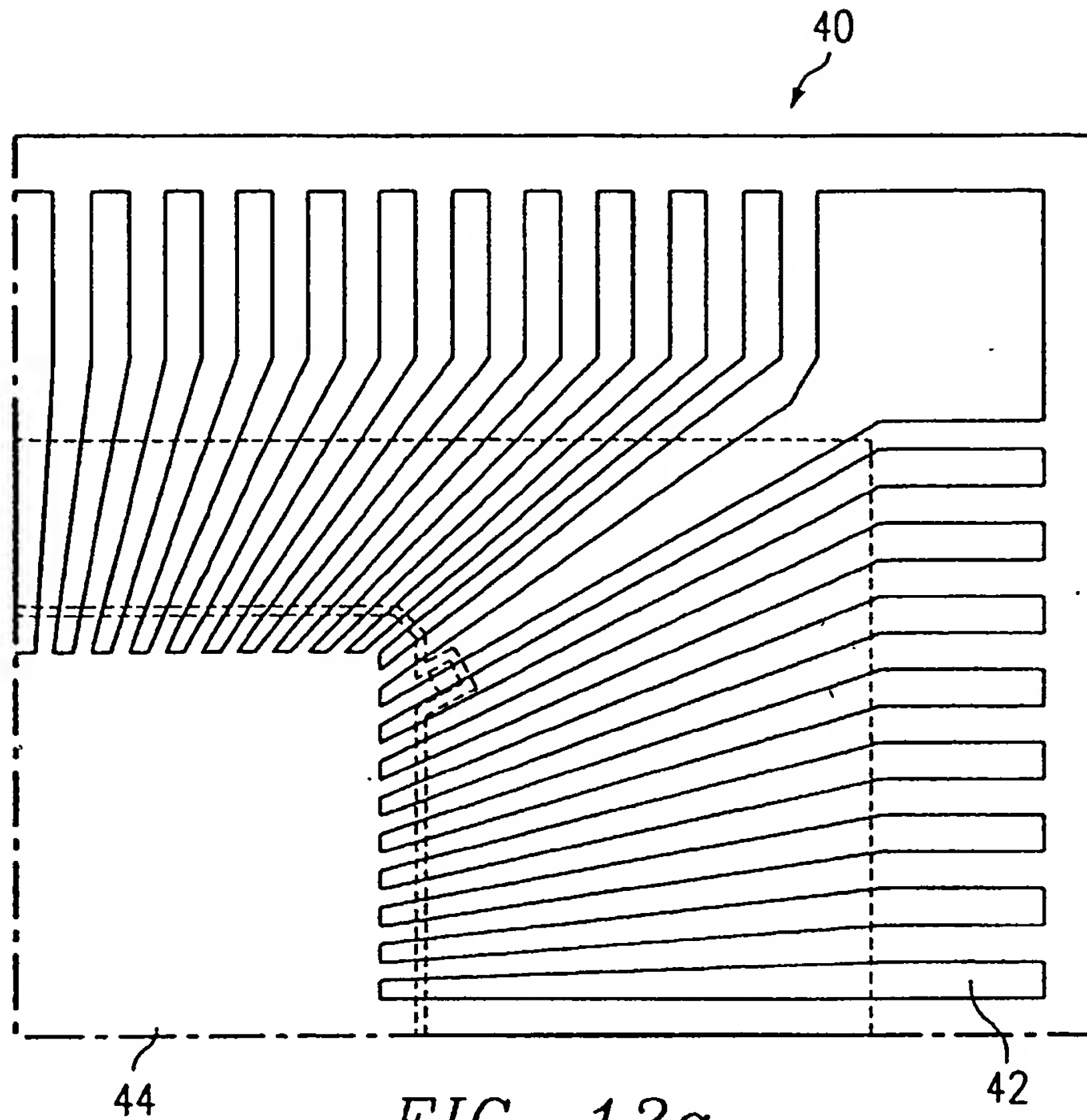
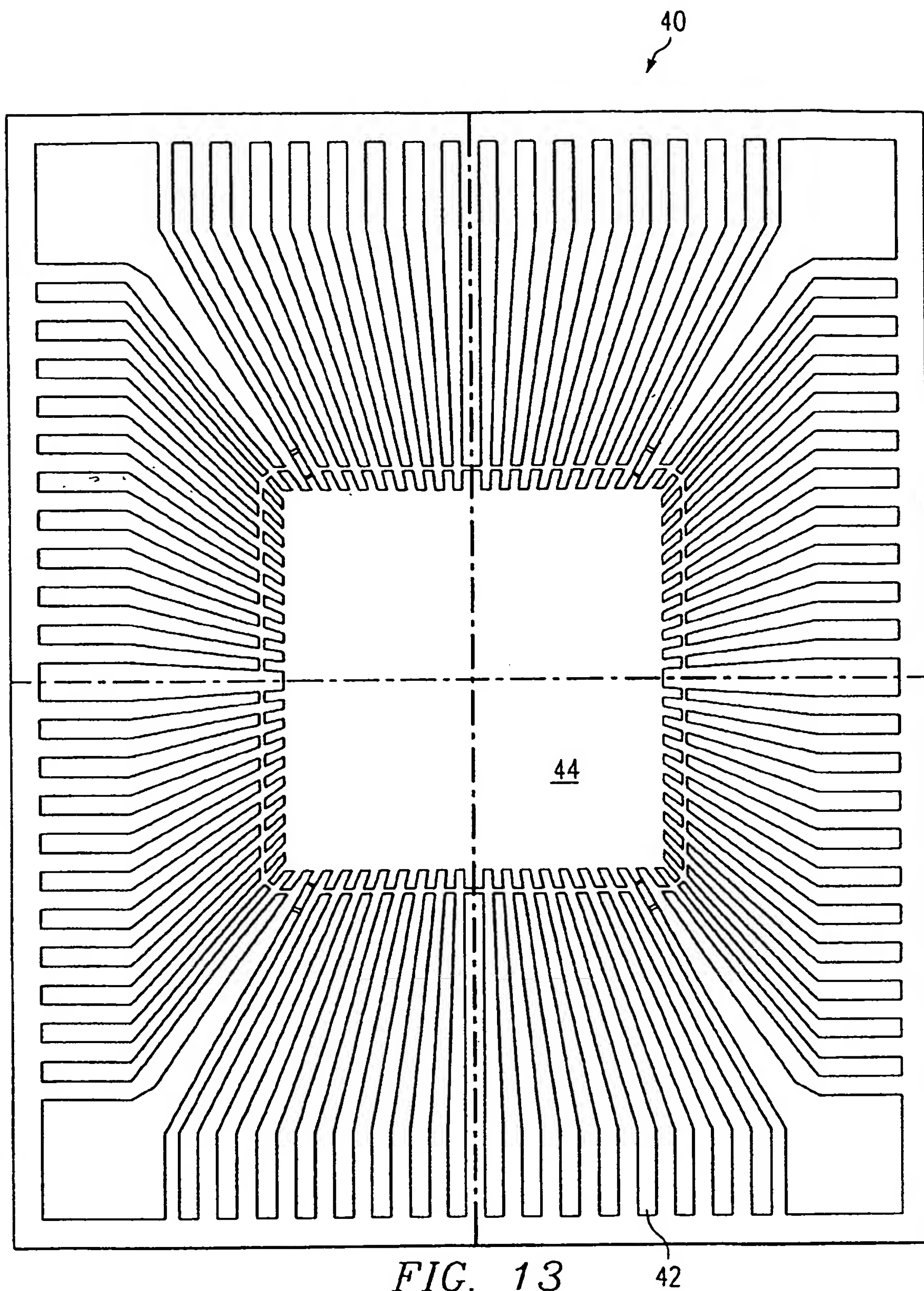


FIG. 11





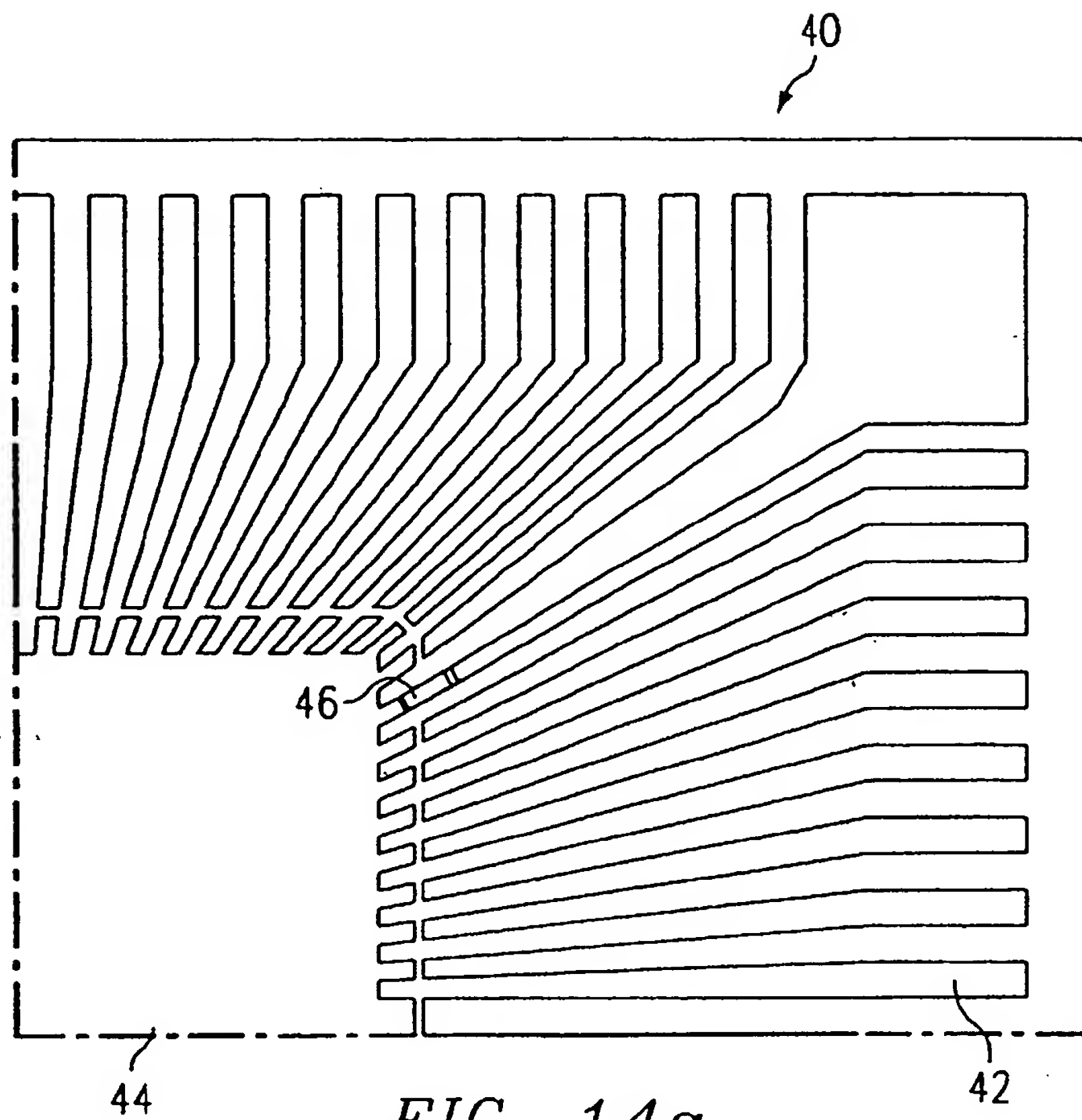


FIG. 14a

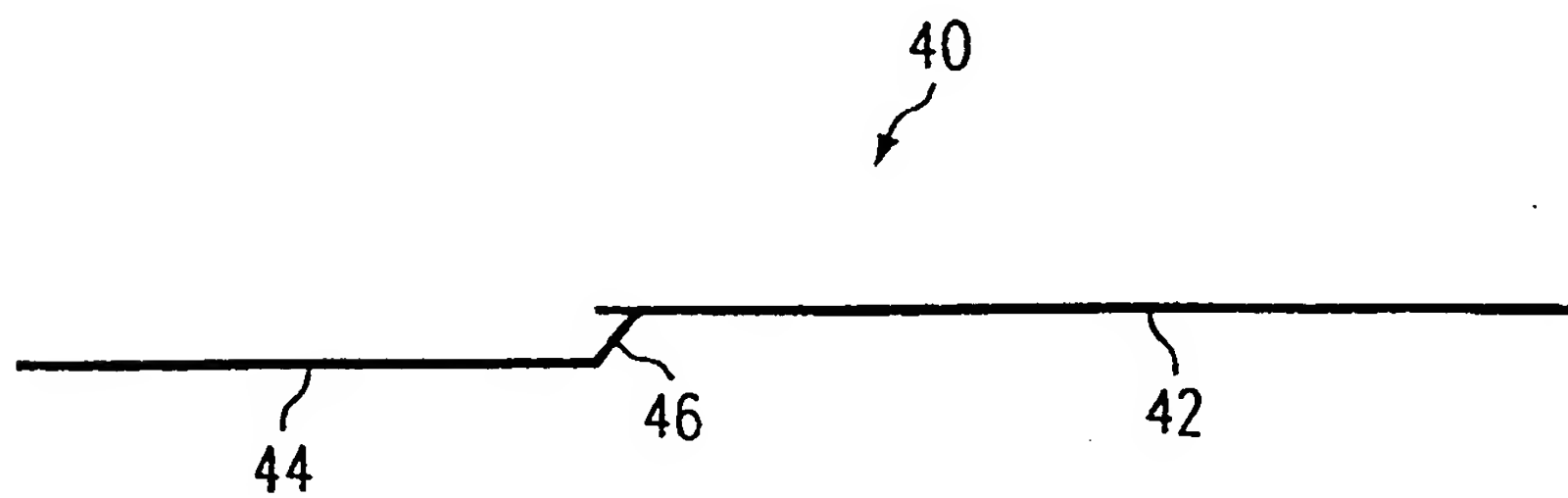


FIG. 14b

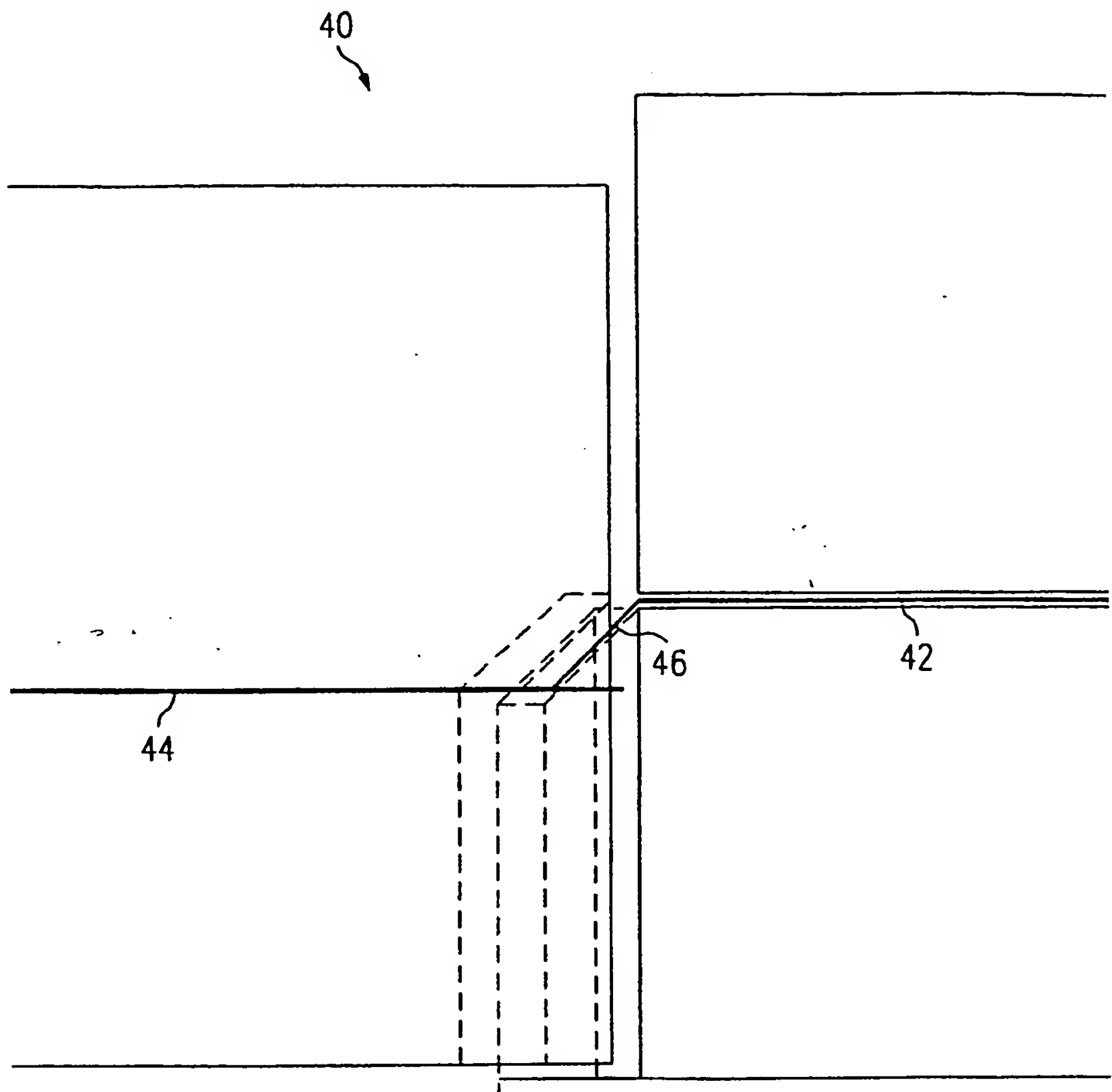


FIG. 15

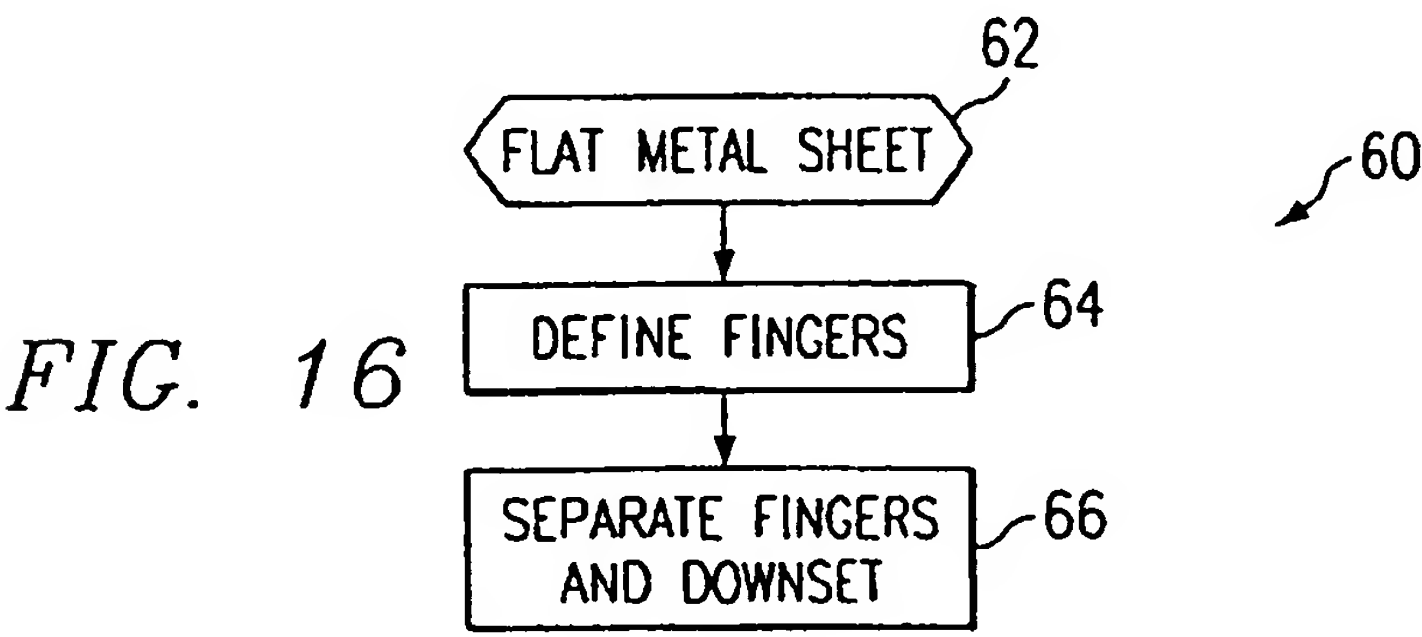


FIG. 16

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11)

EP 0 887 850 A3

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
02.05.2001 Bulletin 2001/18

(51) Int Cl.7: **H01L 21/48, H01L 23/495**

(43) Date of publication A2:
30.12.1998 Bulletin 1998/53

(21) Application number: **98304852.1**

(22) Date of filing: **19.06.1998**

(84) Designated Contracting States:
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE**
Designated Extension States:
AL LT LV MK RO SI

(72) Inventors:
• **Hundt, Michael J.**
Texas 75067 (US)
• **Zhou, Tiao**
Dalles, Texas 75063 (US)

(30) Priority: **23.06.1997 US 880566**

(74) Representative: **Palmer, Roger et al**
PAGE, WHITE & FARRER
54 Doughty Street
London WC1N 2LS (GB)

(71) Applicant: **STMicroelectronics, Inc.**
Carrollton Texas 75006-5039 (US)

(54) Lead-frame forming for improved thermal performance

(57) A lead frame (40) of a plastic integrated circuit package is fabricated in two steps. First, from a rectangular sheet of metal, lead fingers (42) of the lead frame (40) are formed. Second, the die pad (44) of the lead frame (40) is clamped and is simultaneously separated and downset from the lead fingers (42) of the lead frame

(40) by shearing the lead frame with a mated punch die pair (50). Performing the separation and downset of the die pad (44) from the lead fingers (42) results in essentially no horizontal gap between the lead fingers and the die pad (44). The downset of the die pad (44) with respect to the lead fingers (42) results in a vertical separation between the die pad (44) and the lead fingers (42).

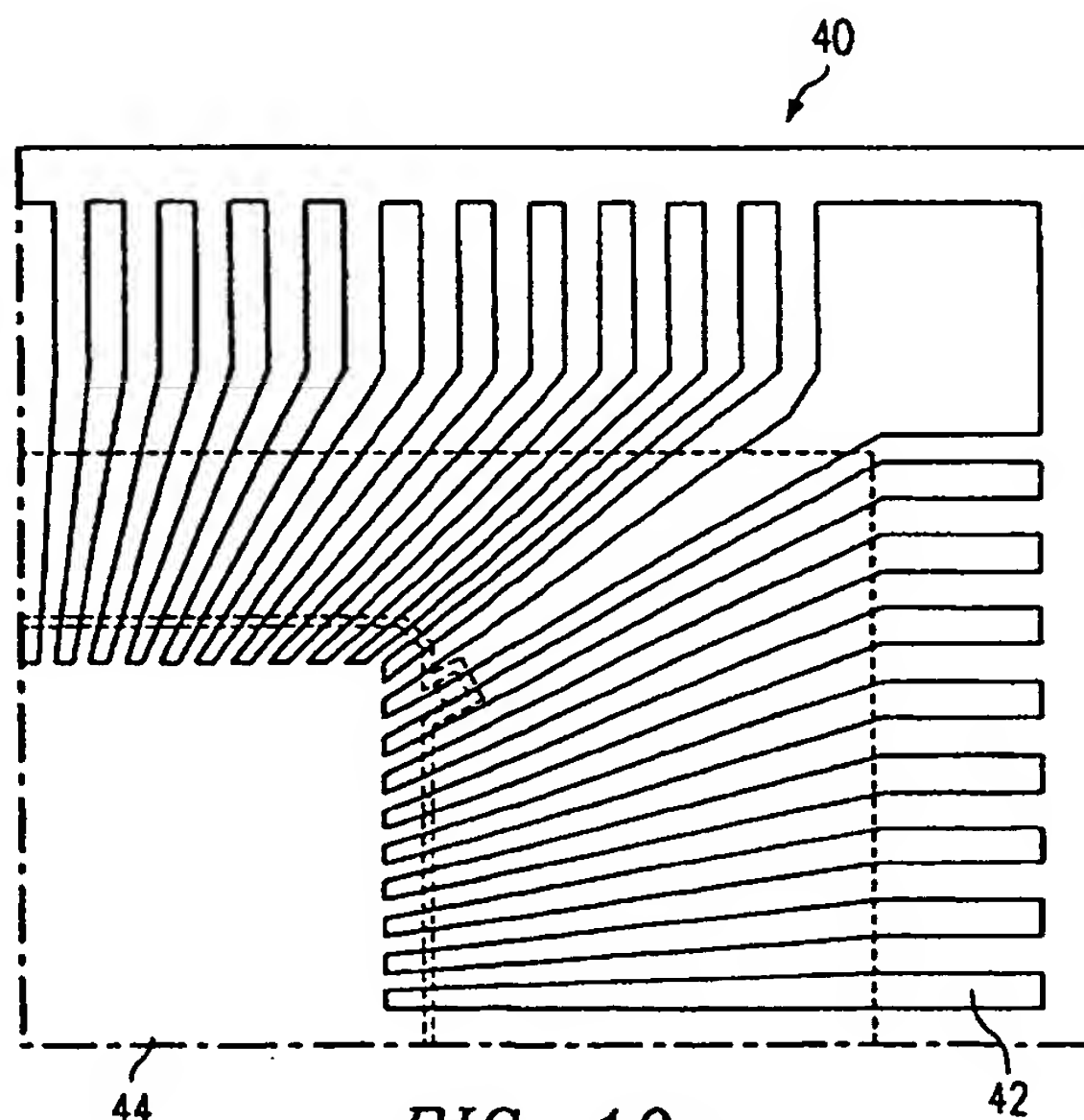
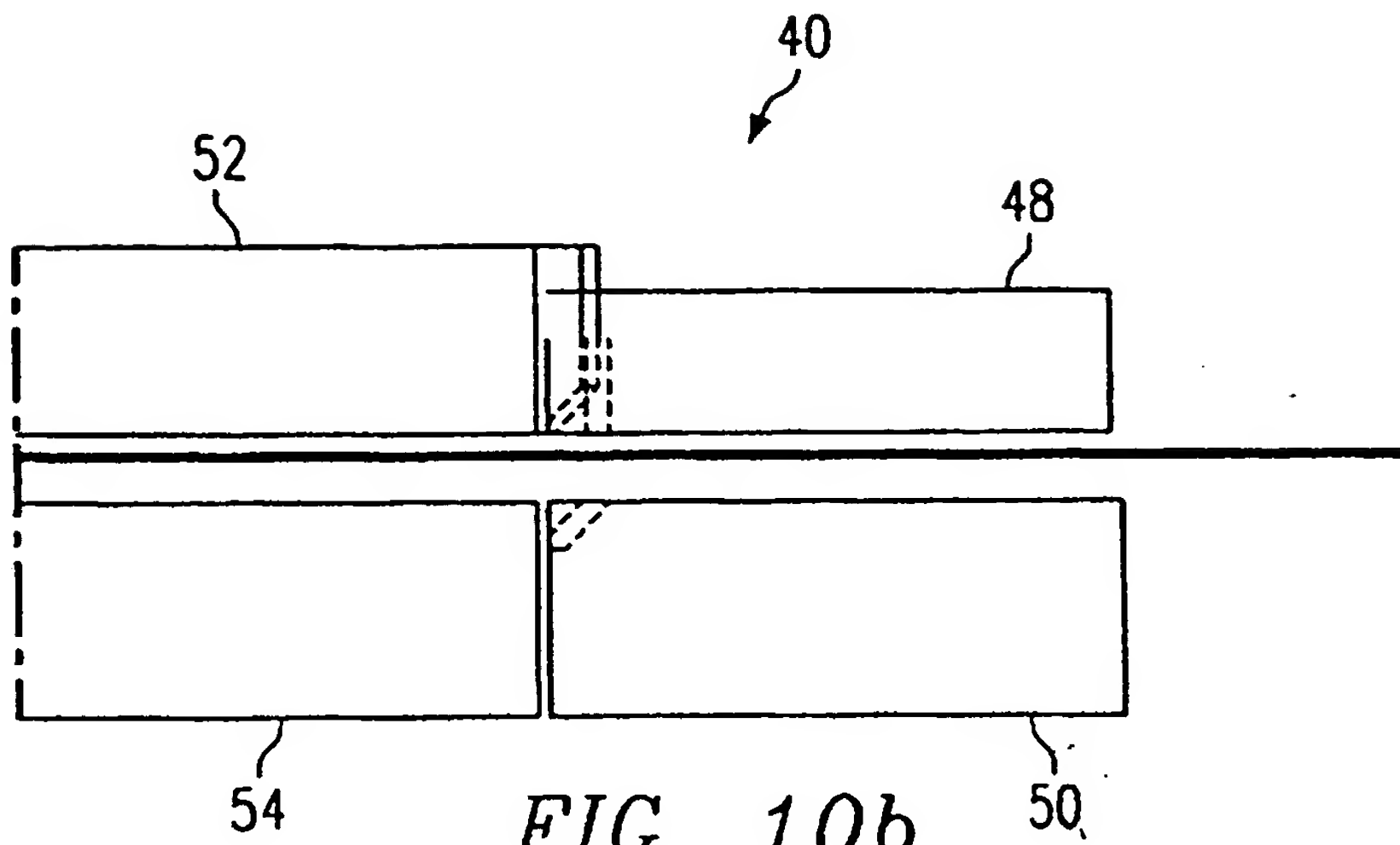


FIG. 10a

EP 0 887 850 A3





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 30 4852

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (InCL6)
X	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 04, 31 May 1995 (1995-05-31) -& JP 07 030038 A (SEIKO EPSON CORP), 31 January 1995 (1995-01-31)	3-7	H01L21/48 H01L23/495
Y	* abstract; figures 3,4 *	1,2	
Y	PATENT ABSTRACTS OF JAPAN vol. 014, no. 479 (E-0992), 18 October 1990 (1990-10-18) -& JP 02 197158 A (DAINIPPON PRINTING CO LTD), 3 August 1990 (1990-08-03) * the whole document *	1,2	
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 397 (E-1120), 8 October 1991 (1991-10-08) -& JP 03 160749 A (NEW JAPAN RADIO CO LTD), 10 July 1991 (1991-07-10)	3-7	
A	* abstract; figures 1A-1C *	1,2	
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 230 (E-1208), 27 May 1992 (1992-05-27) -& JP 04 044255 A (MITSUI HIGH TEC INC), 14 February 1992 (1992-02-14) * the whole document *	1,2	TECHNICAL FIELDS SEARCHED (InCL6) H01L
A	US 4 868 635 A (FRECHETTE RAYMOND A ET AL) 19 September 1989 (1989-09-19) * column 3, line 56 - column 4, line 8; figures 5,6 *	1,2	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 8 March 2001	Examiner Zeisler, P
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03/82 (P/C01)

ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.

EP 98 30 4852

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

08-03-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 07030038 A	31-01-1995	NONE	
JP 02197158 A	03-08-1990	NONE	
JP 03160749 A	10-07-1991	NONE	
JP 04044255 A	14-02-1992	JP 8028449 B	21-03-1996
US 4868635 A	19-09-1989	NONE	